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# FAULT SIMULATOR EVALUATION

University of South Florida

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The fault simulator evaluation study provides rules for relating commercially available fault simulators to a common baseline for calculation of fault coverage. It is known that drastic differences in fault coverage can be obtained from different commercial simulators, yet each bases its calculations on a justifiable and consistent set of rules. The objective of this study was to develop a baseline method of fault simulation and associated rules such that essentially identical results can be obtained by using any commercial simulator product. Four simulators were initially chosen to help develop these guidelines; no simulator among these four is to be considered better than any other simulator. The results of this study have already been put into practice in the form draft MIL-STD-883 Test Method 5012, "Fault Coverage Measurement for Digital Microcircuits."

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## EVALUATION

For digital design, many fault simulators are available in the CAD/CAE tool marketplace. These fault simulators accept as input a logic model (that represents an IC or board) and a sequence of test vectors. They produce as output a list of faults detected by the test vector as well as a number representing the percentage or fraction of faults detected (fault coverage). Recently, specific fault coverage requirements have been demanded for digital ICs intended for military and aerospace use. Discrepancies exist in the results of digital gate level fault simulators which use identical test vectors; one simulator may grade a set of test vectors as having 99% fault coverage while another simulator will grade the same set of test vectors as having only 88% fault coverage. Examples within this report document the drastic differences in fault coverage that may be obtained. In spite of these differences, each simulator bases its calculation on a justifiable and consistent set of rules. The objective of this study was to develop a method of fault simulation and the associated rules such that essentially identical results are obtained by using any gate-level fault simulator. Spurred by the military's reliance upon ASICs, the results of this study would allow the use of any commercial simulator as a tool to provide ASICs that are tested by vector sets with known fault coverages. Although this study was initiated because of the microcircuit testing problem, the results of this study are equally applicable to fault simulation at the board level.

Four simulators were chosen as test cases to develop these guidelines. The results of this study are intended to be applicable to any commercial gate-level fault simulator. This study did not "evaluate" the four fault simulators. Examined were each simulator's fault models, method of fault universe selection, fault collapsing and fault classing. The methods used to correlate the simulators' outputs are described in this final report.

The results presented in this report show that the objectives of the study have been met. The fault levelizing technique described in this report represents a significant step forward in the development of generic qualification procedures. In addition, this effort has already been put in practice in the form of draft MIL-STD-883 Test Procedure 5012, "Fault Coverage Measurement for Digital Microcircuits."

Kevin A. Kwiat

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Project Engineer

# 1. INTRODUCTION

## 1.1 SIMULATION IN CIRCUIT DESIGN

The growth in the performance of LSI/VLSI in recent years has resulted in the development of highly complex computing systems. This, coupled with the fact that many applications now demand error-free computation and performance over long periods of time, has significantly increased required levels of reliability and availability. From the viewpoint of LSI/VLSI product-test preparation, simulation, at least a good circuit (fault-free) simulation, has become an absolute necessity simply because there can be no assurance that a design is structurally or functionally fault-free. Hence, as the system becomes more complex, and more parameters interact in the system, then simulation, which is an imitative process, is used to study the relationships between the parameters [1,2].

## 1.2 WHAT IS SIMULATION?

Simulation is the process of modeling the behavior of an object. Hence, the process of simulation employs models which are an imperfect replica. Therefore, it must be accurate enough to imitate the behavior of the variables in interest in the circuit or system being studied. Generally, digital systems can be described at several levels of abstraction, ranging from the behavioral model to the functional, logic, circuit, and geometric models [1, 3]. However, the level of abstraction studied in this task is at the logic (gate) level.

## 1.3 WHY SIMULATION?

Simulation, as stated earlier, is the process of modeling the behavior of an object. The purpose of using simulation is to save costs by verifying the designs and their specifications. This is possible by allowing design errors to be uncovered and corrected prior to the actual fabrication.

## 1.4 FAULT SIMULATION

Fault simulation of a digital network is the modeling of the network's behavior in the presence of faults which can be caused by physical defects or environmental influences. In addition, fault simulation of logic circuits is an important part of test-generation process. It is used for the purpose of generating fault dictionaries and for verifying the effectiveness of tests. Moreover, fault simulation is a method for measuring or grading the adequacy of a set of test patterns. Fault simulation provides the good machine response to the test, fault coverage, and diagnostic information. The diagnostics relate the failing response states at primary outputs to the assumed faults, and are used to identify process defects or to guide the repair of faulty cells. For VLSI device, acceptable test coverages are usually 95% or greater [4].

## 1.5 FAULT MODELING IN SIMULATION

As stated earlier, the purpose of fault simulation is to find out how good a set of test vectors is at finding manufacturing and field defects in a design. The effectiveness depends on how accurately the fault simulator models the actual faults that could occur on the chip.

Most fault simulators model a manufacturing fault as a condition in which a node is stuck at a logic 1 (s-a-1) or at logic 0

(s-a-0). If a test vector can drive a node of a good circuit to the opposite state from that caused by the defect, and the change in state of that node causes a change of state at a primary output, then the vector detects the presence of that fault. In an actual integrated circuit, however, failures can do more than simply hold a node at Vcc or ground [5]. They can connect two signal lines together (shorts); or disconnect a node (floating). In addition, more than one fault may exist in a circuit at a time. Fortunately, a set of test vectors that covers stuck-at faults (s-a-1 and s-a-0) can also detect most signal line shorts and multiple faults [6].

Floating nodes caused by stuck-open faults are a special problem for fault simulators. To model a floating node, the simulator must be able to model the charge retention (capacitance) of nodes. This can change a combinational circuit into a sequential one [7,8]. Although some simulators claim to test open faults, only stuck-at fault models are considered in this report since it is the common measure of fault coverage.

Since fault simulation depends on the modeling of faults, and since the generation of tests for detecting faults needs to be evaluated for their effectiveness by fault simulation, hence, fault modeling provides a basis for fault-simulation and test-generation.

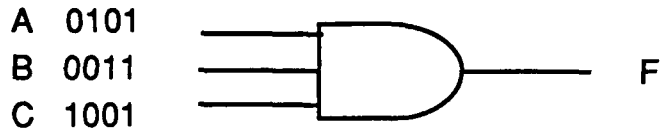
## 1.6 TEST GENERATION

Test generation has become one of the most costly, complicated and time consuming problems in VLSI system design, especially, for Application Specific Integrated Circuits (ASICs). However, it is beyond the scope of this research to generate or develop test sequences using Automatic Test Pattern Generation (ATPG) algorithms. The basic assumption in evaluating the fault simulators, however, is that the test sequence is given (whether derived manually or through an ATPG package) and the identical sequence is used in each fault simulation package.

## 1.7 PROBLEM MOTIVATION

Large computer manufacturers and government agencies (especially for military and aerospace projects) often times require a certain level of fault coverage for a given design. The qualifying activity, however, does not usually require a specific simulator but rather a fault coverage percentage. A recent article in Computer Design (9), issue of June 16, 1988, gives a list of 36 commercial fault simulation systems. Three simulators appearing on this list and selected here are: CADAT, developed by HHB Systems; LASAR, developed by Teradyne; and HILO, developed by Genrad. In addition, HITS, which was developed by the Naval Air Engineering Center, was used in this study.

The real problem in getting different fault coverage values in different simulators when using the same topology and test sequence is due to the way faults are selected, collapsed, simulated and reported. To illustrate this fact, let us take the simple 3 input AND gate shown in Fig. 1. Also, assume the test engineer provides the following test patterns to each simulator: 001,100,010,111. It may be surprising to find out that the fault coverages reported are 57% for CADAT and LASAR, 63% for HITS, and 40% for HILO. Although, the example is very simple and the test sequence is obviously not complete, the point is for even this simple example we had a wide range of fault coverage. One then might ask the following questions: Why do we get these differences in fault coverage evaluation? Are these differences consistent if the circuits are more complex and include sequential elements? How do we know which one is really the right answer, if a right answer really exists? Can these numbers be related to each other? In other words, can one define a standard where all simulators can relate to? These are some of the questions which this study tried to answer.




Fault Coverage For Given Vectors

CADAT = 8/14 = 57%

LASAR = 8/14 = 57%

HITS = 5/8 = 63%

HILO = 2/5 = 40%

Fig. 1 3 - Input AND Gate

## 1.8 PROBLEM APPROACH

Four simulators have been picked for this study. Evaluation of each simulator consists of documenting its general characteristics such as its fault analysis, multiple circuit technologies, user interface, wave-form capability, cell library, fault models, simulation options, fault universe selection, fault classes, and fault collapsing. The investigation of fault collapsing includes fault equivalence and dominance relations which are used to reduce the size of fault lists.

OBJECTIVE: The purpose of the fault simulator evaluation study was to provide rules for relating commercially available fault simulators to a common baseline for calculation of fault coverage. Fault coverage requirements are spelled out in MIL-STD-883 method 5010, "Test Procedures for Custom Monolithic Microcircuits." It is known that drastic differences in fault coverage can be obtained from different commercial-off-the-shelf (COTS) simulators, yet each bases its calculations on a justifiable and consistent set of rules. The objective of this study was to develop a baseline method of fault simulation and associated rules such that essentially-identical results can be obtained by using any COTS simulator product. This will allow the qualifying activity of military microcircuits to "approve" all such commercial tools. The rules shall take into account only easily obtained information about the simulated circuit and shall indicate the range of error. In other words, when rules are applied to the simulators the difference in fault coverage reported by these simulators will be minimal if not zero.

Types and complexity of circuits to be simulated range from a few gates to MSI circuits. It was agreed upon between the research team and RADC that SSI and MSI combinational and sequential circuits were adequate for this study because they have the characteristics of larger circuits (Primary Inputs, Primary Outputs,

fanouts, feedback lines). Once the fundamental rules are obtained, they can be extended to larger circuits. Test patterns were either derived manually or from an ATPG package, or provided to us by RADC. The test sequence were applied to all simulators and the performance of each was evaluated. A set of recommendations and rules for a standard simulator is also proposed.

# 2. FAULT SIMULATOR CHARACTERISTICS

## 2.1. INTRODUCTION

Four simulators have been used in this study, they are:

1) CADAT: Version 5.2, HHB Systems.
2) LASAR: Version 6.2, Teradyne.
3) HILO: Version 3.1, Genrad.
4) HITS: Version 13, Naval Air Engineering Center.

The following features for these simulators have been outlined and documented elsewhere. However, for the purpose of this study, only parts f through j are explained.

a) Introduction and Features
b) Primitives and Libraries
c) Technologies Supported
d) Nodal Contentions, Internal States and Strengths
e) Fault models and algorithm
f) Fault Universe Selection
g) Fault Selection for Simulation
h) Fault Collapsing/equivalence
i) Fault Coverage Computation
j) Potential Faults Handling

All four simulators use the concurrent fault simulation algorithm which has become the most widely used method [1]. Concurrent simulation is a one-pass process and in most cases requires less calculation than serial, parallel or deductive fault simulation. Significantly reducing the number of gate calculations makes fault simulation much faster. The tradeoff, however, is that concurrent simulation is a memory intensive algorithm. All simulators ran on MICROVAX 2000 running VMS operating system.

## 2.2 FEATURES:

### 2.2.1 FAULT UNIVERSE SELECTION:

#### 2.2.1.1 CADAT:

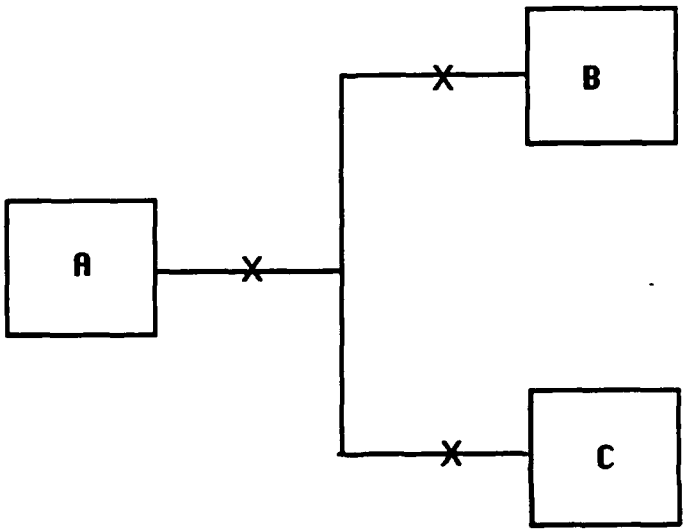
The fault universe (the total set of faults which can be considered) consists of faults from the following five categories:

a) output pin faults
b) input pin faults
c) internal output faults
d) internal input faults
e) internal state faults (ex. ROM, RAM, serial shift register primitives).

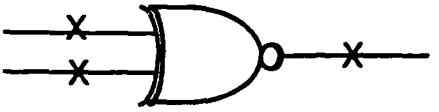
EXAMPLES:

Each X in the diagrams represents SA0 and SA1.

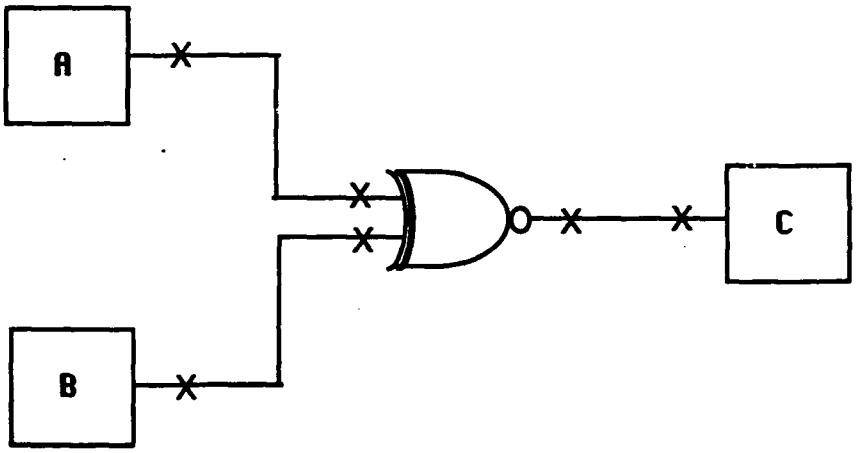
1) General fanout, all technologies:



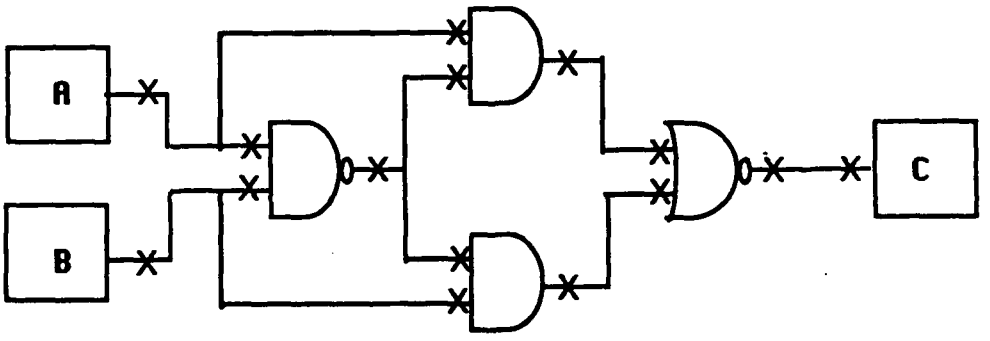
2) XNOR as a primitive, alone:



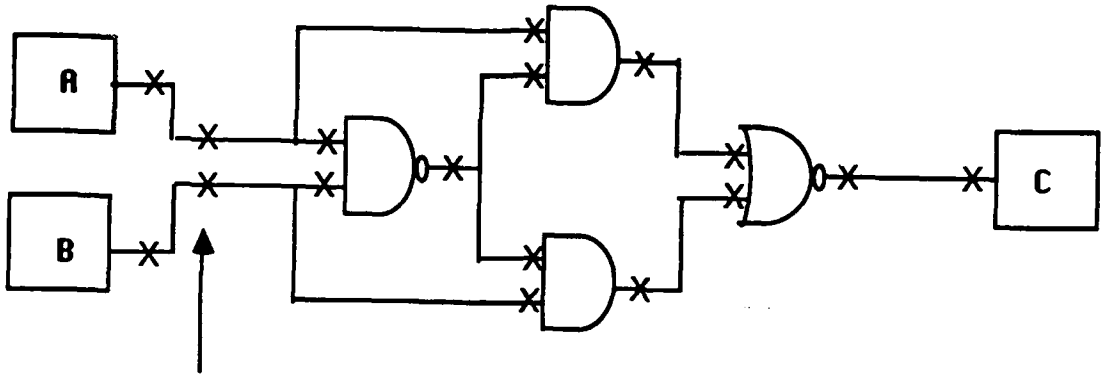
3) XNOR as a primitive, in a circuit:




4) XNOR expanded, in a circuit:



5) XNOR as an internal macro, in a circuit:




The arrow above shows a characteristic of CADAT: for each PI (A,B) with no fanout, 2 faults (each in a separate class) are considered per PI. C is the PO.

2.2.1.2 LASAR:

Faults are selected through two different simulators Faultput and Efaults as follows:

Through Faultput; the following faults can be chosen:

- s1. user pins stuck at 0 and 1.
- s2. all nodes stuck at 0 and 1.
- s3. component nodes stuck at 0 and 1.
- s4. open fault any node.
- s5. short between any nodes.
- s6. any node can be selected for stuck at 0, 1 or open.

Through Efaults, the following faults can be introduced:

- N node's primitive outputs stuck at 1 and 0.
- J primitive outputs and inputs stuck at 1 and 0.
- C NMOS and PMOS primitives stuck on or off, other nodes stuck at 0 or 1.
- M includes class C plus inputs of non-MOS primitives stuck 0 or 1.

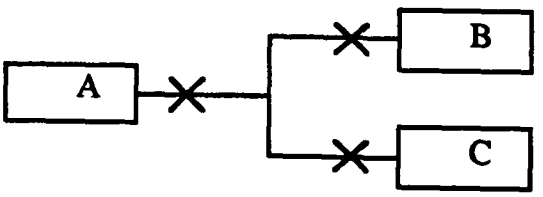
Note that stuck-open for MOS technology is included.

In summary any type of fault that can be thought of can be introduced in LASAR either through Faultput or through Efaults. However, the Efaults selection is limited.

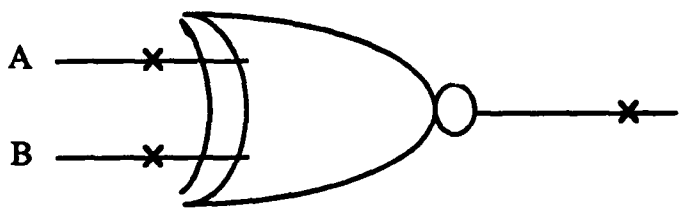
EXAMPLES:

Each X in the diagram represents SA0 and SA1.

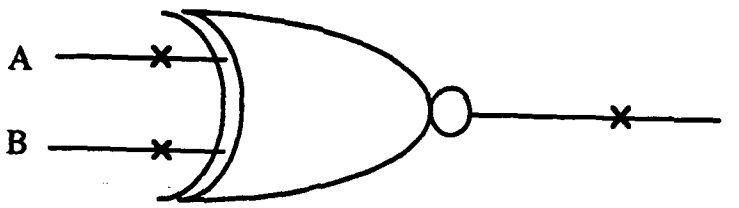
1. General fanout, all technologies:



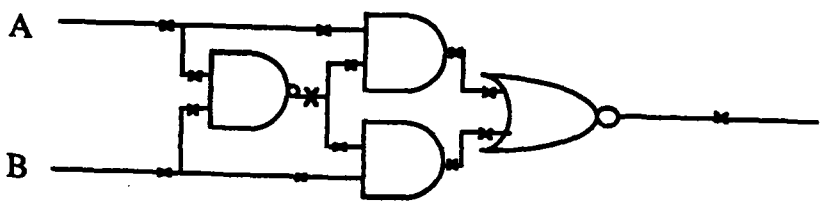

2. XNOR as a primitive, alone:



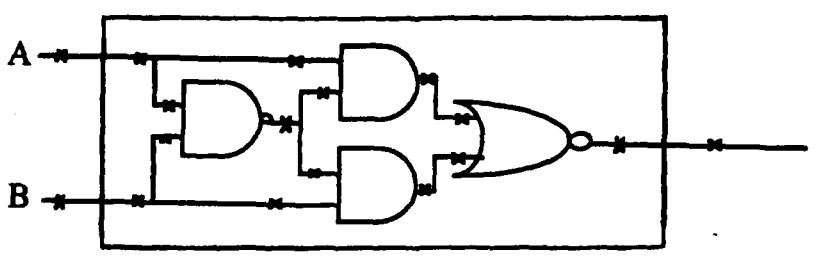
3. XNOR as a primitive, in a circuit:




4. XNOR expanded, in a circuit:




5. XNOR as a macro, in a circuit:



2.2.1.3 HILO

The following faults or any subset may be chosen:

- s0 Default.
- s1 Primary inputs SA0 and SA1.
- s2 Primary outputs SA0 and SA1.
- s3 Gate model input terminals OPEN0 and OPEN1.
- s4 Gate model output terminals DRIVE0 and DRIVE1.
- s5 Gate model output terminals DRIVEZ.
- s6 Gate model wires SA0 and SA1.
- s7 Gate model wires SHORT.
- s8 gate model SUPPLY1 (Vcc) SA0 and SUPPLY0 (GND) SA1.
- s9 Functional model wires and registers SA0 and SA1.
- s10 Functional model wires SHORT.
- s11 Functional model INHIBIT.

The default fault-set (s0) includes the following faults:

s1, s2, s6, s8, and s9.
OPEN1 for AND and NAND gates.
OPEN0 for OR and NOR gates.
OPEN0 and OPEN1 for buffers, inverters, and transmission gates.

All these fault subsets are available to any level of circuit hierarchy.

In top-level circuit, the user can select:
Any single subset or all subsets which are available in the circuits.
Any number of faults within the selected subsets.
When no faults are specified, the default fault-set (s0) is selected automatically by HILO.

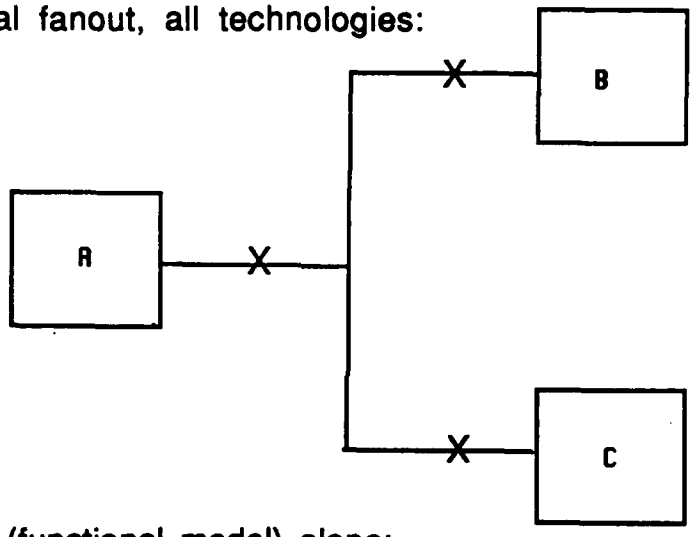
Exception: Subset s4 always merges to SA fault when both specified in a circuit. In sub-level circuit, the user can select similar fault-sets as top-level, except subsets s1 and s2, i.e. user can select any internal faults but the boundary faults in a sub-level

circuit for HILO considers the two connected wires (one in the top level circuit and the other in the sub-level circuit) as a single physical wire and only one pair of SA faults are injected.

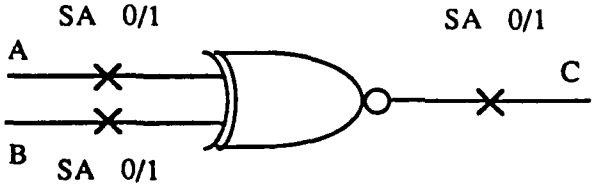
EXAMPLES:

The following examples show how the faults are selected by HILO-3 when s1, s2, s3, s6, s9, fault-sets are specified (all STUCK-AT and OPEN faults).

1). General fanout, all technologies:

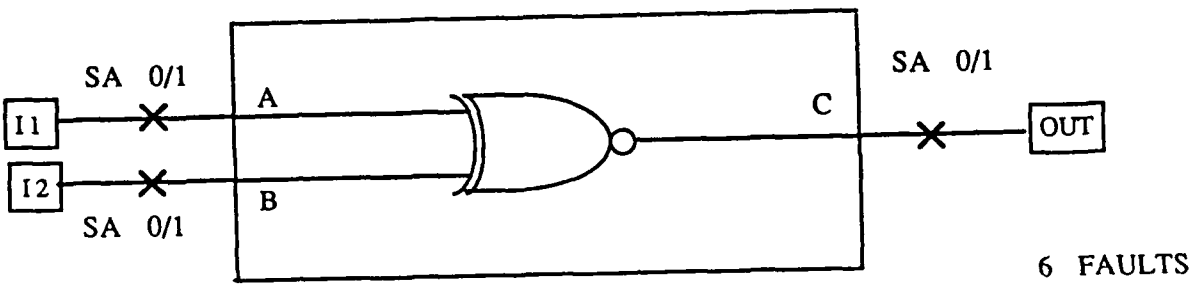



2). XNOR (functional model) alone:

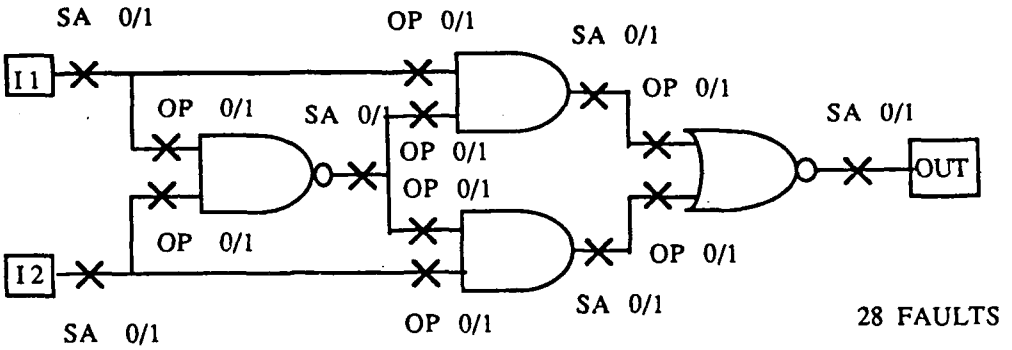



6 FAULTS

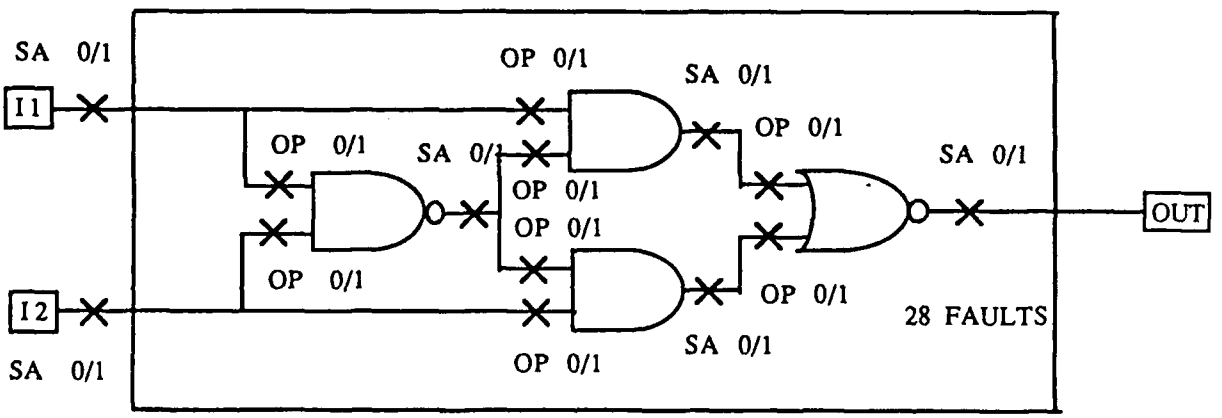
3). XNOR (functional model) in a circuit:




4). XNOR (gate model ) at top-level:




5). XNOR (gate model) at sub-level:



2.2.1.4 HITS

All nodes stuck-at are first read without any exclusion. These faults are composed of all inputs, outputs and internals, except primitive internals, then the simulator starts dropping certain faults before forming classes. The examples cited in HILO also apply for HITS for 1,2 and 3. However, examples 4 and 5 are shown in subsection 2.2.3.4.

2.2.2 FAULT SELECTION FOR SIMULATION:

2.2.2.1 CADAT

CADAT allows great flexibility in the selection of subsets of faults to be considered in a fault simulation. Any number of faults from the total universe to a single fault can be selected. Standard selections are one or more of the five categories of the fault universe, or a single specified fault (single fault simulation). In addition, the user can create a file containing the faults to be selected (selective faulting). Faults that are to be excluded from a simulation can be specified in the circuit description. Finally, the user can specify the simulation of a random subset of the faults.

2.2.2.2 LASAR:

Faults can be selected as all nodes, components, inputs and outputs of components stuck at zero or one, and outputs stuck at 0 and 1, Shorts between nodes and open any particular inputs. Fault simulation features:

- Selectable number of faults per pass.
- Stuck-At 0, 1 input, open, and Bridging faults.
- Incremental fault simulation.
- Detailed fault diagnostic dictionary generation.

2.2.2.3 HILO

Fault simulation features:

Parallel Value List (PVL) algorithm.
Selectable number of faults per pass.
Stuck-At 0, 1 and Bridging faults.
Incremental fault simulation.
Detailed fault diagnostic dictionary generation.

2.2.2.4 HITS

The process of fault selection consists of the following:

1) Removing indistinguishable failures from considerations.
2) Grouping the detectable failures into equivalent classes, and 3) selecting a representative failure for each class; the closest to the primary output.

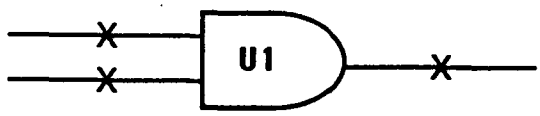
2.2.3 FAULT COLLAPSING AND EQUIVALENCE:

2.2.3.1 CADAT

Faults that affect a network in a similar manner are considered equal and placed in an equivalence class. Only one fault from an equivalence class is actually simulated. If that fault is detected all faults in the class are considered detected. These equivalence classes are technology-independent. For each primitive in a network, both input and output faults are considered. External connections however, are considered separate devices (a bus by default) and faults on these are placed in separate equivalence classes. This feature is unique only to CADAT. There is no direct information about which particular fault from an equivalence class is being simulated.

EXAMPLES: BASIC PRIMITIVES:

1) AND gate:




6 faults

4 equivalence classes:

U1.1/0,U1.2/0, U1.Y/0

U1.1/1

U1.2/1

U1.Y/1

(ex. U1.Y/1: Unit 1, Output Y s-a-1)

2) NAND gate:


6 faults

4 equivalence classes:

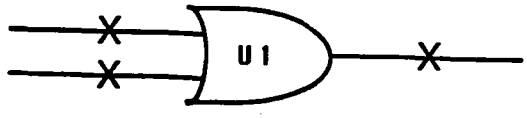
U1.1/0, U1.2/0, U1.Y/1

U1.1/1

U1.2/1

U1.Y/0

3) OR gate:




6 faults

4 equivalence classes:

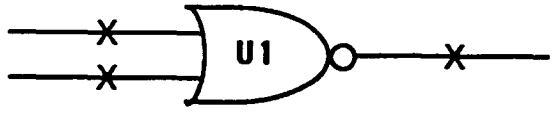
U1.1/1,U1.2/1, U1.Y/1

U1.1/0

U1.2/0

U1.Y/0

4) NOR gate:




6 faults

4 equivalence classes:

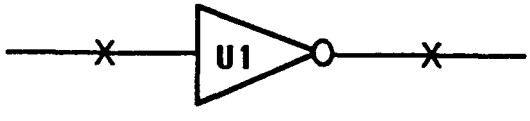
U1.1/1, U1.2/1,U1.Y/0

U1.1/0

U1.2/0

U1.Y/1

5) INVERTER, alone:




4 faults

2 equivalence classes:

U1.1/1, U1.Y/0

U1.1/0, U1.Y/1

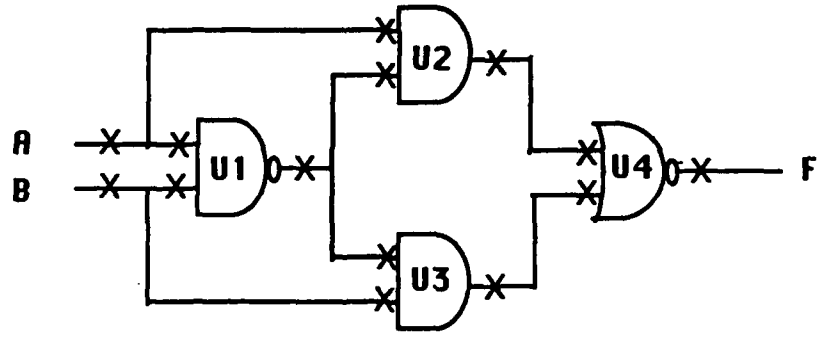
Primary inputs are put in classes by themselves in CADAT and their respective faults are not collapsed even if no fanouts exist. For example, for the AND gate in 1), if 2 primary inputs exist, then, there will be 10 faults and 8 classes (the 4 equivalence classes mentioned and A/0,B/0,A/1and B/1).

6) XNOR, expanded, with externals:

28 faults

16 equivalence classes:

A/1
B/1
U2.A0/1
U2.Y/1, U3.Y/1, U4.A0/1, U4.A1/1, U4.Y/0
U3.A1/1
B/0
U1.AO/1
U1.Y/0
U3.A0/0, U3.A1/0, U3.Y/0, U4.A1/0
U4.Y/1
A/O
U1.A1/1
U2.A0/0, U2.A1/0, U2.Y/0, U4.A0/0
U1.A0/0, U1.A1/0, U1.Y/1
U2.A1/1
U3.AO/1



2.2.8.2 LASAR:

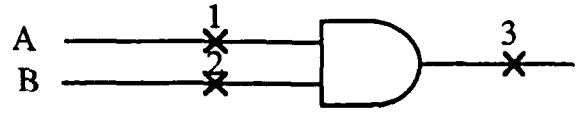
Equivalent faults are collapsed into single class and LASAR picks up one fault only from each class for fault simulation. The faults which can be collapsed are the equivalent faults which depend on the type of elements and the configuration of the circuit as shown in the examples below.

EXAMPLES: BASIC PRIMITIVES:

1) AND gate: 4 classes, 10 faults

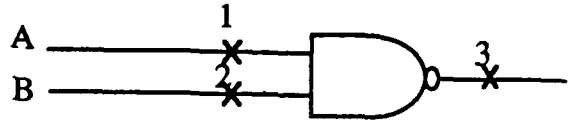
1. A@0;B@0;3@0;1@0;2@0
2. A@1;1@1
3. B@1;2@1
4. 3@1

(ex. 2@1: line 2 s-a-1)



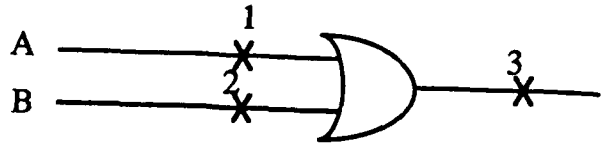

2) NAND gate: 4 classes, 10 faults

1. 1@0;3@1;A@0;3@0;B@0
2. A@1;1@1
3. B@1;2@1
4. 3@0



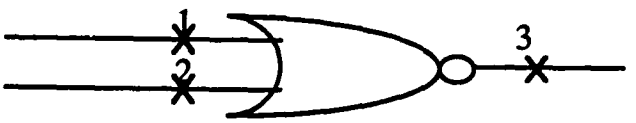

3) OR gate: 4 classes, 10 faults

1. 1@0;A@0
2. 1@1; 3@1; A@1;B@1;2@1
3. 2@0;B@0
4. 3@0



4) NOR gate: 4 classes, 10 faults

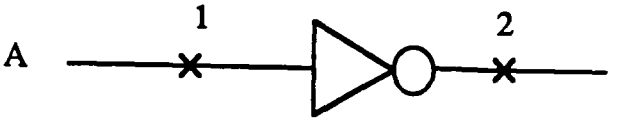
1. 1@0;A@0
2. 1@1;3@0;A@1;B@1;2@1
3. 2@0; B@0
4. 3@1



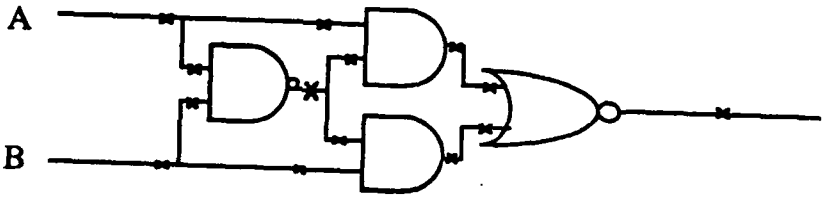

The primary input faults collapse at the gate input faults if no fanout exists in LASAR.

5) INVERTER: 4 faults, 2 classes

1. 1@0;2@1; A@0
2. 1@1;2@0;A@1




6) XNOR, expanded, with externals:



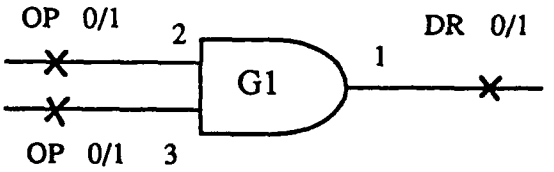
| CLASS | FAULTS |
|---|---|
| 1 | A@0 |
| 2 | A@1 |
| 3 | B@0 |
| 4 | B@1 |
| 5 | 1P3@0 |
| 6 | 1P3@1,1P1@0,1P2@0 |
| 7 | 2P3@0,4P2@0,2P2@0,2P1@0 |
| 8 | 2P3@1,4P1@0,4P2@1,4P3@1,2P6@1 |
| 9 | 2P6@0,4P3@0,2P4@0,2P5@0 |
| 10 | 4P1@1 |
| 11 | 1P1@1 |
| 12 | 1P2@1 |
| 13 | 2P1@1 |
| 14 | 2P2@1 |
| 15 | 2P4@2 |
| 16 | 2P5@1 |
| SUMMARY | Total number of faults: 28 |
| | Total number of classes: 16 |

2.2.3.3 HILO

Equivalent faults are collapsed into a single class and HILO picks up one fault only from each class for fault simulation. The faults which can be collapsed depend on the type of elements and the configuration of the circuit.

EXAMPLES: BASIC PRIMITIVES

1) AND gate: 6 faults, 4 classes

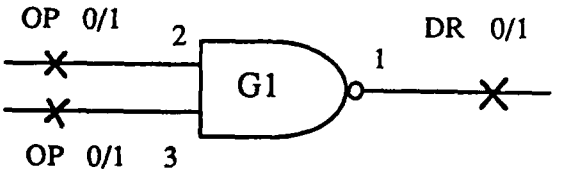



| CLASS | FAULT |
|---|---|
| 1 | G1.1/DR0, G1.2/OP0, G1.3/OP0 |
| 2 | G1.1/DR1 |
| 3 | G1.2/OP1 |
| 4 | G1.3/OP1 |

(ex. G1.1/DR0: Gate 1, Output line s-a-0)

---

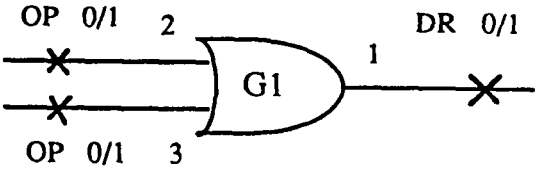
2) NAND gate: 6 faults, 4 classes




| CLASS | FAULT |
|---|---|
| 1 | G1.1/DR1, G1.2/OP0, G1,3/OP0 |
| 2 | G1.1/DR0 |
| 3 | G1.2/OP1 |
| 4 | G1.3/OP1 |

---

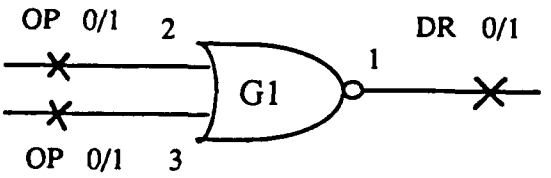
3) OR gate: 6 faults, 4 classes




| CLASS | FAULT |
|---|---|
| 1 | G1.1/DR0 |
| 2 | G1.2/OP0 |
| 3 | G1.3/OP0 |
| 4 | G1.1/DR1,G1.2/OP1, G1.3/OP1 |

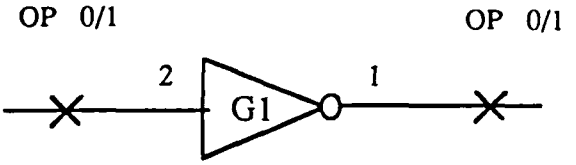
---

4) NOR gate: 6 faults, 4 classes




| CLASS | FAULT |
|---|---|
| 1 | G1.1/DR1 |
| 2 | G1.2/OP0 |
| 3 | G1.3/OP0 |
| 4 | G1.1/DR0, G1.2/OP1, G1.3/OP1 |

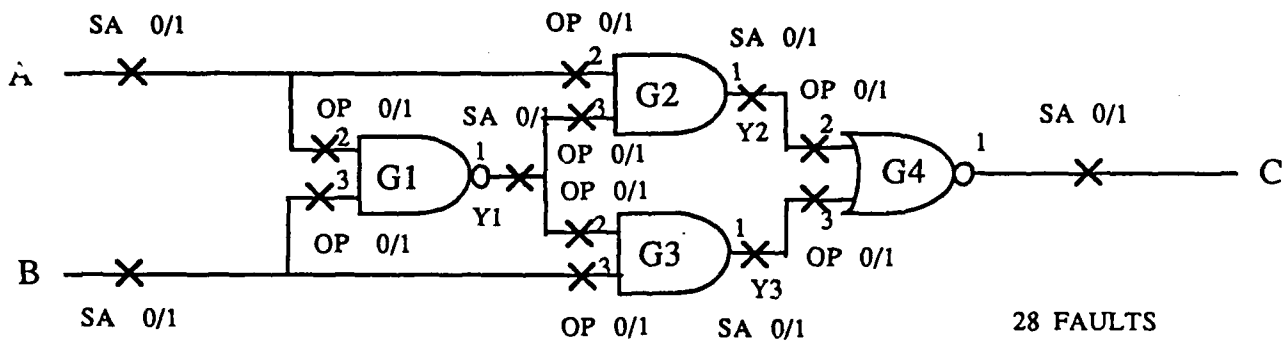
5) NOT gate: 4 faults, 2 classes




| CLASS | FAULT |
|---|---|
| 1 | G1.1/DR0, G1.2/OP1 |
| 2 | G1.1/DR1, G1.2/OP0 |

In HILO the primary input faults also collapse to the gate input faults when no fanout points exist at the primary input.

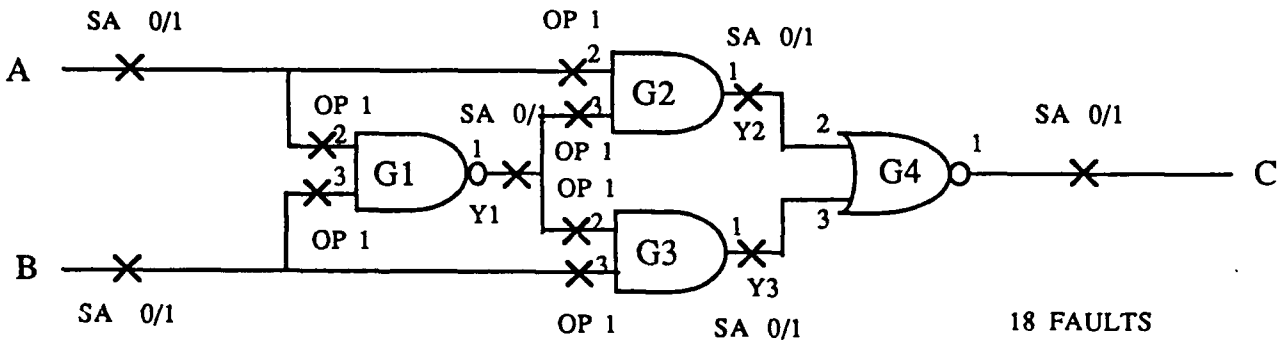
6a) XNOR with all STUCK and OPEN faults specified:




| CLASS | FAULTS |
|---|---|
| 1 | G3.3/OP1 |
| 2 | G3.2/OP1 |
| 3 | G3.2/OP0, G3.3/OP0, G4.3/OP0, Y3/SA0 |
| 4 | G2.3/OP1 |
| 5 | G2.2/OP1 |
| 6 | G2.2/OP0, G2.3/OP0, G4.2/OP0, Y2/SA0 |
| 7 | G1.3/OP1 |
| 8 | G1.2/OP1 |
| 9 | Y3/SA1, C/SA0, Y2/SA1, G4.2/OP1, G4.3/OP1 |
| 10 | Y1/SA1, G1.2/OP0, G1.3/OP0 |
| 11 | Y1/SA0 |
| 12 | C/SA1 |
| 13 | B/SA1 |
| 14 | B/SA0 |
| 15 | A/SA1 |
| 16 | A/SA0 |

SUMMARY Total number of faults: 28
Total number of classes: 16

6.b) XNOR with DEFAULT fault-set specified:




| CLASS | FAULTS |
|---|---|
| 1 | G3.3/OP1 |
| 2 | G3.2/OP1 |
| 3 | Y3/SA0 |
| 4 | G2.3/OP1 |
| 5 | G2.2/OP1 |
| 6 | Y2/SA0 |
| 7 | G1.3/OP1 |
| 8 | G1.2/OP1 |
| 9 | Y3/SA1, C/SA0, Y2/SA1 |
| 10 | Y1/SA1 |
| 11 | Y1/SA0 |
| 12 | C/SA1 |
| 13 | B/SA1 |
| 14 | B/SA0 |
| 15 | A/SA1 |
| 16 | A/SA0 |

SUMMARY Total number of faults: 18
Total number of classes: 16

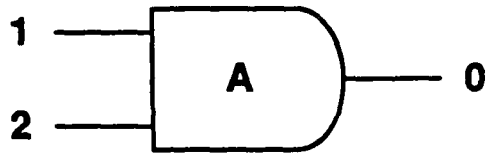
In HILO, some faults are removed due to technology when the default fault set is specified as shown in ex. 6.b.

2.2.3.4 HITS:

HITS form the classes after excluding redundant faults, because of technology behavior and because of single source-single sink network (fault collapsing). For this reason one expects to see different classes for different technologies.

EXAMPLES: BASIC PRIMITIVES:

1)AND

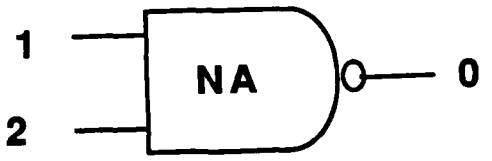



| CLASS | PIN | STUCK AT |
|---|---|---|
| 1 | A-1 | SA/0 |
| 1 | A-2 | SA/0 |
| 1 | A-0 | SA/0 |
| 2 | A-1 | SA/1 |
| 3 | A-2 | SA/1 |
| 4 | A-0 | SA/1 |

# of faults = 6

# of equivalence classes = 4

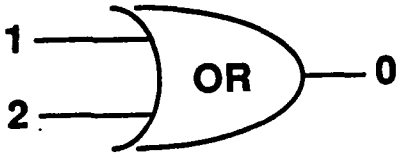
2) NAND




| CLASS | PIN | STUCK AT |
|---|---|---|
| 1 | NA-1 | SA/0 |
| 1 | NA-2 | SA/0 |
| 1 | NA-0 | SA/1 |
| 2 | NA-0 | SA/0 |
| 3 | NA-1 | SA/1 |
| 4 | NA-2 | SA/1 |

# of faults = 6
# of equivalence classes = 4

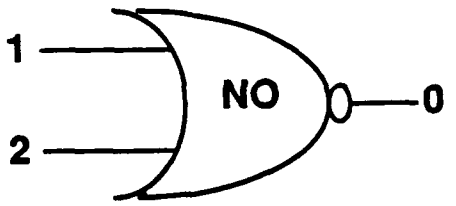
3) OR




| CLASS | PIN | STUCK AT |
|---|---|---|
| 1 | OR-1 | SA/1 |
| 1 | OR-2 | SA/1 |
| 1 | OR-0 | SA/1 |
| 2 | OR-1 | SA/0 |
| 3 | OR-2 | SA/0 |
| 4 | OR-0 | SA/0 |

# of faults = 6
# of equivalence classes = 4

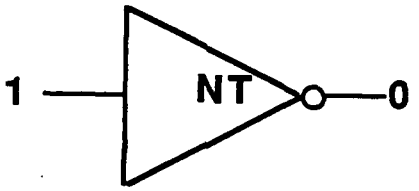
4) NOR




| CLASS | PIN | STUCK AT |
|---|---|---|
| 1 | NO-1 | SA/1 |
| 1 | NO-2 | SA/1 |
| 1 | NO-0 | SA/0 |
| 2 | NO-1 | SA/0 |
| 3 | NO-2 | SA/0 |
| 4 | NO-0 | SA/1 |

# of faults = 6
# of equivalence classes = 4

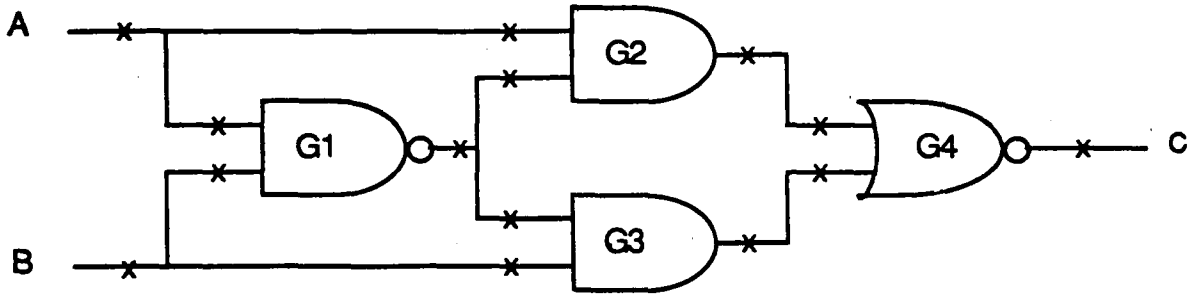
5) INV




| CLASS | PIN | STUCK AT |
|---|---|---|
| 1 | NT-1 | SA/0 |
| 1 | NT-0 | SA/1 |
| 2 | NT-1 | SA/1 |
| 2 | NT-0 | SA/0 |

# of faults = 4
# of equivalence classes = 2

6) XNOR




CMOS: 28 Faults, 16 Classes
ECL: 18 Faults, 16 Classes
TTL: 18 Faults, 16 Classes

Classes are the same as the other simulators, Fig. 3.1, p. 43.

In HITS, faults due to primary inputs are collapsed to gate input faults when no fanouts exist at primary inputs.

The swapper module as stated before will form the classes but will remove the following types of faults:

1) Those not swapped in (excluded).
2) Those with no output path.
3) Those with locked at attributes.

and 4) Technology dependent and due to fault collapsing.

The closest fault to the primary output is always selected to represent the class for simulation.

HITS is very technology dependent as far as fault collapsing is concerned. The following example shows the results in three different technologies for the same 2-bit adder circuit.

TWO-BIT ADDER

| STEP | # OF FAULTS | | | % OF DETECTION | | | # OF CLASSES DETECTED | | |
|---|---|---|---|---|---|---|---|---|---|
| | TTL | ECL | CMOS | TTL | ECL | CMOS | TTL | ECL | CMOS |
| 1 | 15 | 23 | 25 | 32.6 | 50.0 | 40.3 | 15 | 19 | 21 |
| 2 | 19 | 13 | 20 | 73.9 | 78.3 | 72.6 | 15 | 9 | 16 |
| 3 | 1 | 0 | 1 | 76.1 | 78.3 | 74.2 | 1 | 0 | 1 |
| 4 | 5 | 3 | 6 | 87.0 | 84.8 | 83.9 | 5 | 3 | 6 |
| 5 | 4 | 4 | 6 | 95.7 | 93.5 | 93.6 | 4 | 2 | 4 |
| 6 | 2 | 3 | 4 | 100 | 100 | 100 | 2 | 1 | 2 |

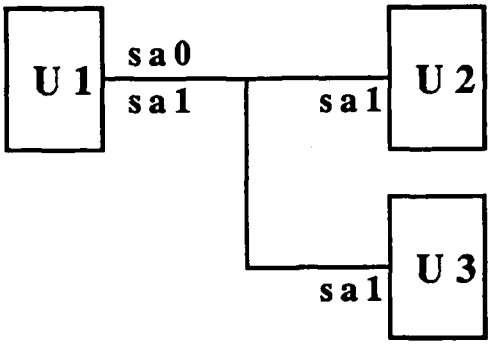
| | TTL | ECL | CMOS | | TTL | ECL | CMOS |
|---|---|---|---|---|---|---|---|
| # faults detect | 46 | 46 | 62 | classes detect | 42 | 34 | 50 |
| # faults undetect | 0 | 0 | 0 | classes undetect | 0 | 0 | 0 |
| # total faults | 46 | 46 | 62 | total classes | 42 | 34 | 50 |

It is evident from the above example that HITS would define the fault universe depending on the technology that is declared and the swapper option that is chosen by the user.

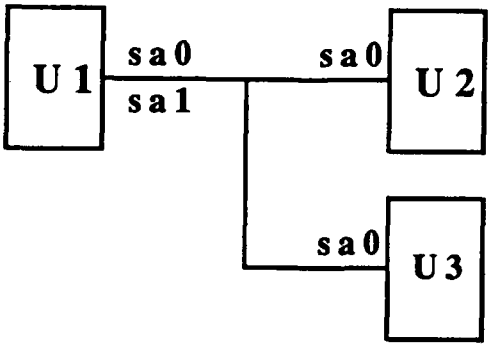
The rules used in removing some faults from the fault list due to technology in HITS are given below:

a) Single Source - Multiple Sink

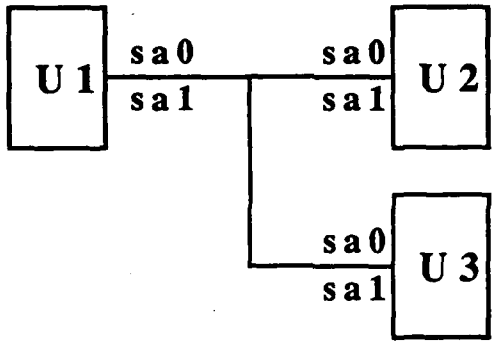
i) For TTL technology, the fault insertion rules exclude the sink SA0 faults of "single source - multiple sink" nets.




ii) For ECL technology, the fault insertion rules exclude the sink SA1 faults of "single source - multiple sink" nets.

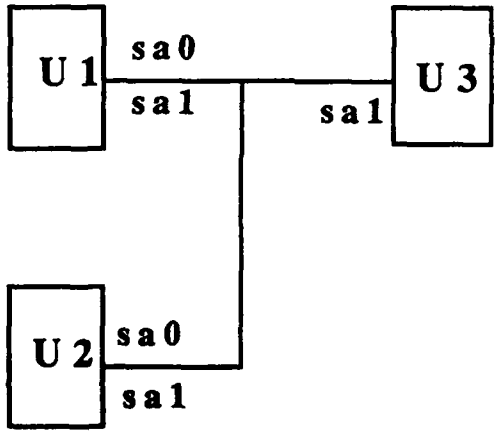


iii) For CMOS technology, the fault insertion rules include the sink faults of "single source - multiple sink" nets.

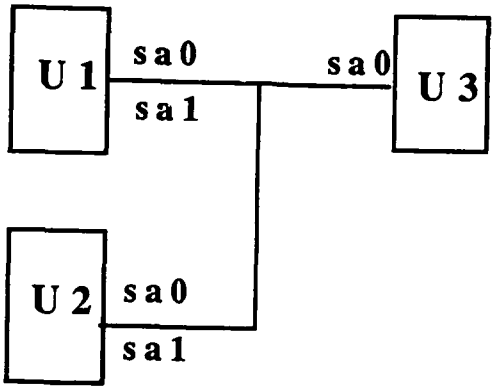



b) Multiple Source - Single/Multiple Sink:

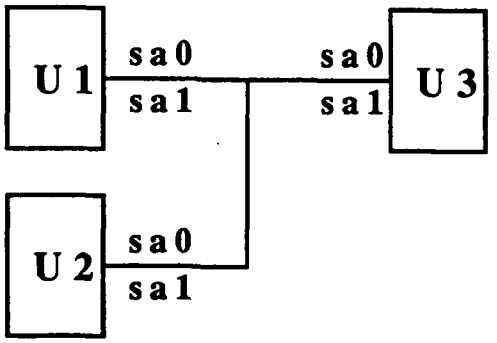
i) For TTL technology, the fault insertion rules exclude the sink SA0 fault(s) of "multiple source - single/multiple sink" nets.



ii) For ECL technology, the fault insertion rules exclude the sink SA1 fault(s) of "multiple source - single/multiple sink" nets.




iii) For CMOS technology, the fault insertion rules include the sink faults of "multiple source - single/multiple sink" nets.




Note the CMOS fault insertion rules is what the other simulators use for all technologies; i.e. all faults are injected. This difference seems to be very important in fault simulation using HITS.

2.2.4 FAULT COVERAGE:

2.2.4.1 CADAT

In CADAT the fault detection percentage is calculated as the ratio of total faults detected to total faults simulated. The coverage is given as a range, from a pessimistic lower limit (solid detections only) to an optimistic upper limit (potential detections (if any) added to the solid detections).

A second detection percentage which is based on standard statistical methods is also provided. This projected detection estimates the minimum probable detection rate for the full fault set based on the observed detection rate.

2.2.4.2 LASAR

LASAR uses the number of faults for the P.C. (percentage coverage) calculation as follows:

$$P.C. = \frac{\text{The number of faults detected}}{\text{The total number of faults}} \times 100$$

LASAR also gives a range from solid detections only to solid plus potential detections when potential detects exist.

2.2.4.3 HILO

HILO uses the number of fault classes for the P.C. calculation

$$P.C. = \frac{\text{The number of fault classes detected}}{\text{The number of fault classes simulated}} \times 100$$

The number of fault classes simulated is equal to the total number of fault classes minus the number of undetectable fault classes. Potential faults are also available in HILO.

HILO defines the following two types faults as undetectable:

1) The fault which has no path to the primary output, such as VCC/SA0 and GND/SA1 in single IC chip simulation.
2) The fault which has a path to the primary output but it is blocked out by locking one of the primary inputs to VCC or GND.

2.2.4.4 HITS:

In HITS the fault detection percentage is calculated as the ratio of total faults detected to the total detectable faults (after removing faults mentioned in 2.2.2.4). No potential detection is available.

2.2.5 POTENTIAL FAULTS HANDLING

CADAT, LASAR, and HILO can handle potential (or possible detects). Potential detects are very important especially with using clock lines in sequential circuits. In combinational networks, CADAT and LASAR report potential detection when using open - collector gates. However, HILO considers open - collector faults as either weak 0 or weak 1. Hence, HILO results give solid detection (strength is weak 1, which is just above the threshold, and weak 0, which is just below the threshold). HITS has no ability for potential detection and reports pessimistic values (i.e. no credit is given to potential detects). However, it claims to detect open-collector faults which gives, in this case, an optimistic value.

# 3. FAULT SIMULATION EVALUATION

## 3.1 STRATEGY

The key to evaluate the four fault simulators is to use several test cases under the same conditions and observe the output nodes for each test vector. The objective, here, is not to choose one of the simulators and declare it superior over the others, but rather to evaluate each simulator and arrive at a standard set of rules that can give a better correlation between all the simulators. In other words, we need to do the following:

a) understand the differences in these simulators, as was done in the previous chapter, in terms of fault injection, classing and collapsing, evaluation of fault coverage figure, etc.

b) devise a standard simulator where one can have a unified approach to fault injection, classes, fault collapsing and fault coverage evaluation.

c) compare the fault coverage - as our figure of merit - of each simulator to the proposed standard simulator and compute the margin of error after it is defined.

## 3.2 TEST CASES

Several circuits have been simulated to perform this study. In fact ten circuits were chosen where five were combinational circuits and five were sequential circuits. These circuits are:

A. Combinational

1. Exclusive NOR
2. Two-Bit ADDER
3. Gray Code Converter
4. Comparator (SN 7485)
5. ALU (LS 74181)

B. Sequential

1. Edge Triggered D flip-flop
2. Two D flip-flop and AND gate
3. Four Cascaded D flip-flops
4. Four-bit Counter (74163)
5. Four-bit Shifter (74195)

These circuits were picked for different reasons. First, it was decided that no large or complex circuits would be used since no new information would be gained with the amount of effort needed to analyze such circuits. Secondly, these circuits were diversified. For instance, the exclusive NOR circuit was built using basic primitives and the fan-out points were observed for fault injections and classes. For example,the number of faults and the process of fault removal in the fault list in HITS was observed as shown in Fig. 3.1. However, in the two-bit adder, the XOR (exclusive OR) gate was used as a primitive. Since this primitive is not available in HILO, buffers were used at the inputs of the macro to block the faults in the macro cell equivalent to XOR gate. The Gray Code Converter shows an example of a circuit where an input line was connected to ground, and therefore some faults cannot be detected. The comparator and the ALU examples illustrate a relatively complex and multi-level circuit. In addition, the open-collector output in the ALU was tested. Both the expanded and unexpanded (i.e. macro cell and primitive) circuits in the ALU were tested. Some of these results are explained in the following sections.

For the sequential circuits, many different examples were also used. First, an edge-triggered D flip-flop was used where the clock line is basically a controlled input with combinational elements and feedback lines. Also, this example had two undetected faults, since no test vector can detect these faults due to contradictory assignments. The second example also had an interesting phenomenon of how faults are classified in the different simulators and also illustrated some undetectable faults. The four cascaded D

flip-flops network was an example of how drastically some of the simulators may differ from each other for no apparent reason! This will be addressed when these results are presented. The counter and shifter examples again illustrate reasonable MSI type circuits with sequential elements.

Most of the test patterns for simulating all faults in these circuits were obtained either manually or through an ATPG package. However, some were supplied by the government (7485,74181). The method of analyzing these circuits is outlined below:

1) Obtain the topology of the circuit and enter the circuit to each simulator. Some of the primitives did not exist in some of the simulators. Therefore, a macro cell was created to perform the function of the primitive and buffers were created to block fault injections inside the macro cells (i.e. only boundary faults at these macros were considered).

2) Apply all test vectors in the same order to all simulators and observe the process of fault detection at each step of the test pattern application.

3) Observe the number of faults detected per step, the number of classes detected per step, and compute the cumulative fault coverage figure at each step. The solid detections, potential detections and the undetected faults are also reported. The cumulative standard coverage was computed by hand and a margin of error was also computed to show the difference between the current evaluation of fault coverages and the proposed standard fault coverage evaluation.

4) After observing and analyzing all the results, a set of characteristics or rules for correlating these fault simulators were obtained. These rules will be discussed in the following chapter. However, in order to understand the results which are shown in this

chapter, two main conclusions are discussed here. The cumulative standard fault coverage evaluation and the margin of error concept.

First, it was shown in Chapter 1, Fig. 1, that when simulating the 3-input AND gate, we had 3 different fault coverage figures for the given test pattern. This is mainly due to the way faults are injected and the way the fault coverage is computed. It is probably not acceptable that the fault coverage is 63% when A/1, B/1 and C/1 are not covered. All these faults are unique faults. Similarly, because of the way fault classes and equivalent faults are classified we had another figure which is also optimistic at 57%. It is proposed that the fault coverage which is the ultimate figure in evaluating and verifying circuits be defined in terms of the unique faults or fault classes rather than total faults injected in the circuit. The conceptual reasoning behind this will be explained in the following chapter. Hence, the cumulative standard fault coverage is computed as follows:

$$FC\% = \frac{\text{Number of fault classes detected}}{\text{Total number of fault classes}} \times 100$$

It is shown in the results that the difference in the performance of these fault simulators is minimized. This difference is called the margin of error. This figure of merit is defined as a range between the minimum distance (or difference) between any two simulators to the maximum distance (difference) between any two simulators. Observing this margin of error (MOE) number before and after using the proposed standard fault coverage figure should indicate how these simulators are correlated and how close or far from the actual fault coverage figure these simulators are.

## 3.3 SIMULATION RESULTS

Ten circuits were simulated for this evaluation, and the result of each circuit is given in this section. For each circuit, the same

conditions were applied for each simulator. However, in the case of HILO, the XOR gate is not a primitive and has to be built as a macro. In addition, LASAR does not have primitive flip-flops but rather a FF chips library. Hence, more faults are considered. These differences will be pointed out when they occur and some recommendations on how to minimize such differences will be given in the next chapter.

### 3.3.1 COMBINATIONAL CIRCUITS:

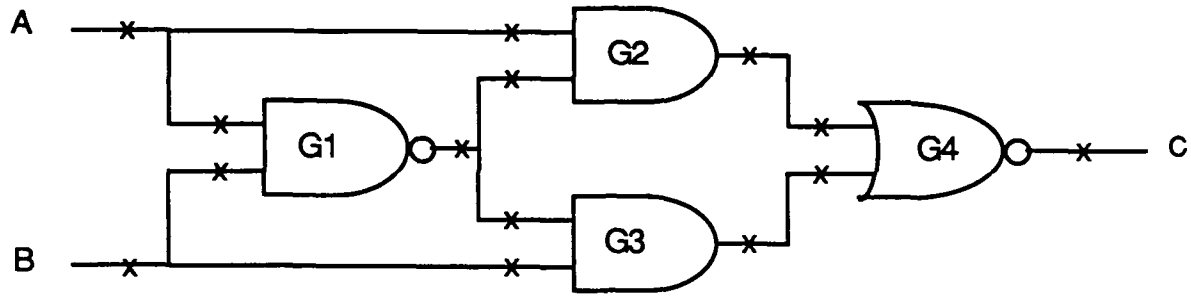
#### 3.3.1.1 XNOR CIRCUIT:

Fig.3.1 shows the XNOR circuit simulated. The number of total faults in this circuit is 28 faults. However, if the declared technology in HITS is TTL, the total number of faults in HITS is 18 faults. This is due to the process of fault removal in HITS. This process in HITS is as follows:

For a fanout only, all s/0 faults are removed, and for a non-fanout all s/0 and s/1 faults are removed. Only faults underlined in Fig. 3.1 are considered in TTL implementation in HITS. All Tables show the number of test vectors (steps), the number of faults and classes detected per step, the cumulative fault coverage as given by each simulator, the standard fault coverage and margin of error (MOE) as defined in the previous section.

In addition, the total number of faults detected (solid and/or potential) and undetected are listed. In some Tables, there will be two columns for HITS to represent both TTL and CMOS.

Table 3.2 and Fig. 3.2 illustrate the MOE when the fault coverage of each simulator is evaluated and after the standard fault coverage is evaluated. It is very clear that the MOE, when the fault coverage is calculated using fault classes, is zero, since most simulators, although they use different fault injection procedures, have the same fault collapsing techniques. Fig.3.2 also shows the min-max (difference between any two simulators) which is the MOE.




Total : 28 faults ( HITS : total 18 faults for TTL )

Classes

| | |
|---|---|
| A/0 | G2.1/0, G2.2/0, G2.3/0, G4.1/0 |
| A/1 | G2.1/1 |
| B/0 | G2.2/1 |
| B/1 | G2.3/1, G4.1/1, G4.3/0, G3.3/1, G4.2/1 |
| G1.1/0, G1.2/0, G1.3/1 | G3.1/0, G3.2/0, G3.3/0, G4.2/0 |
| G1.1/1 | G3.1/1 |
| G1.2/1 | G3.2/1 |
| G1.3/0 | G4.3/1 |

Fig. 3.1 XNOR ( Expanded )

(1,2 : Inputs, 3 : Output)

## Table 3.1 XNOR (EXHAUSTIVE VECTORS)

| Step | Number Faults Detected/step LASAR | CADAT | HITS | HILO | Number Classes Detected/step LASAR | CADAT | HITS | HILO | Cumulative Coverage (%) LASAR | CADAT | HITS | HILO | MOE | Cumulative Standard Coverage LASAR | CADAT | HITS | HILO | MOE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 9 | 9 | 7 | 9 | 5 | 5 | 5 | 5 | 32.1 | 32.1 | 38.9 | 31.2 | 0.0-7.7 | 31.2 | 31.2 | 31.2 | 31. | 0-0 |
| 2 | 8 | 8 | 5 | 8 | 5 | 5 | 5 | 5 | 60.7 | 60.7 | 66.7 | 62.5 | 0.0-6.0 | 62.5 | 62.5 | 62.5 | 62.5 | 0-0 |
| 3 | 6 | 6 | 3 | 6 | 3 | 3 | 3 | 3 | 82.1 | 82.1 | 83.3 | 81.2 | 0.0-2.1 | 81.2 | 81.2 | 81.2 | 81.2 | 0-0 |
| 4 | 5 | 5 | 3 | 5 | 3 | 3 | 3 | 3 | 100.0 | 100.0 | 100.0 | 100.0 | 0-0 | 100.0 | 100.0 | 100.0 | 100.0 | 0-0 |

| Faults: | LASAR | CADAT | HITS | HILO | Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|---|---|---|---|---|
| Solid Detections: | 28 | 28 | 18 | 28 | Solid Detections: | 16 | 16 | 16 | 16 |
| Potential Detections: | 0 | 0 | 0 | 0 | Potential Detections: | 0 | 0 | 0 | 0 |
| Undetected: | 0 | 0 | 0 | 0 | Undetected: | 0 | 0 | 0 | 0 |
| Total: | 28 | 28 | 18 | 28 | Total: | 16 | 16 | 16 | 16 |



## Table 3.2 XNOR (EXHAUSTIVE VECTORS)

| STEP | MOE BEFORE (%) | MOE AFTER (%) |
|---|---|---|
| 1 | 0.0-7.7 | 0.0-0.0 |
| 2 | 0.0-6.0 | 0.0-0.0 |
| 3 | 0.0-2.1 | 0.0-0.0 |
| 4 | 0.0-0.0 | 0.0-0.0 |

MARGIN OF ERROR BEFOR AND AFTER APPLICATION OF STANDARD FAULT COVERAGE (SFC)

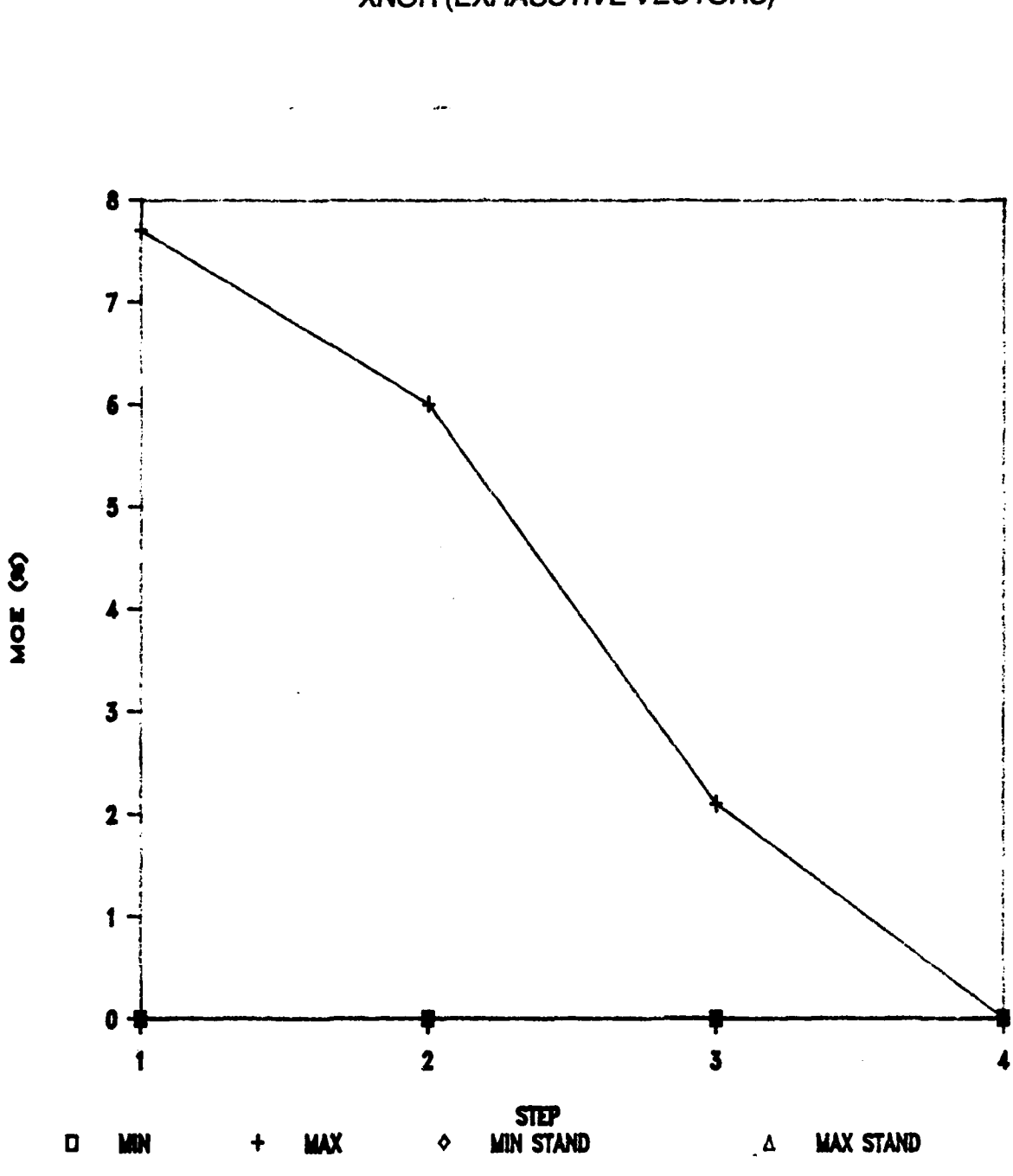

XNOR (EXHAUSTIVE VECTORS)
MOE (SE)
8
7
6
5
4
3
2
1
0
1
2
3
4
STEP
MIN
MAX
MIN STAND
MAX STAND

Fig. 3.2

While there is a huge difference in fault coverage calculated normally, this difference is zero when the standard calculation is used. The procedure for calculating the standard fault coverage in each simulator will given in Chapter 4.

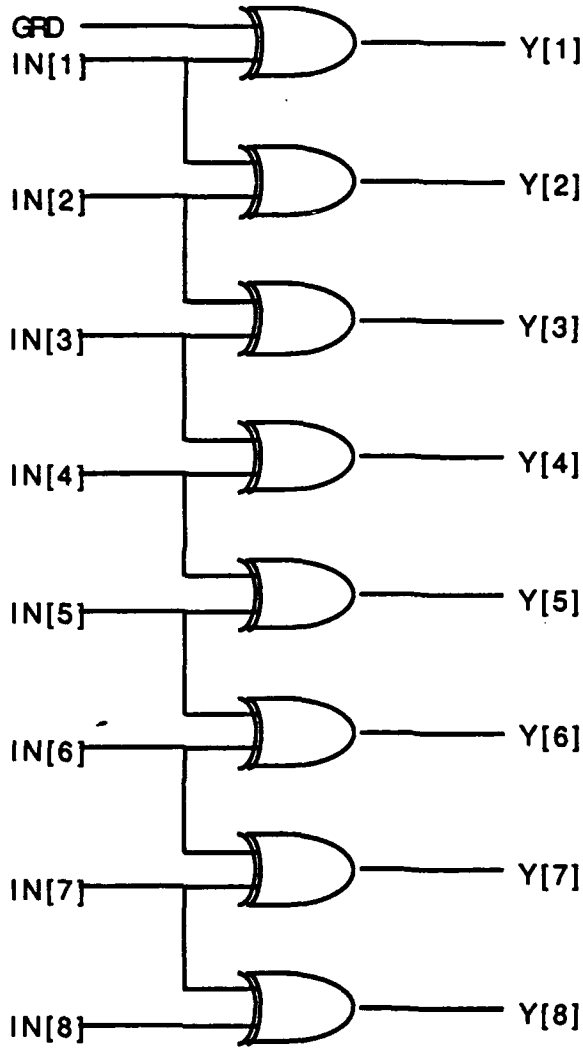
3.3.1.2 GRAY CODE CONVERTER:

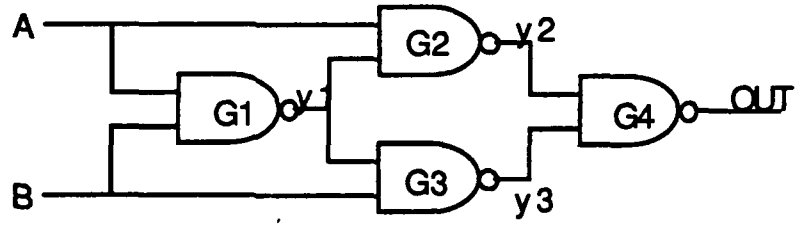
Fig 3.3 shows the circuit diagram for the Gray Code Converter. Table 3.3 shows the simulated results for this circuit. The MOE is clearly smaller when the standard coverage calculation is used. This is illustrated in Table 3.4 and Fig. 3.4. Also, it must be mentioned that HITS gives an optimistic value since faults due to the ground pin are removed from the fault list. Hence, when HITS is omitted in the analysis, the MOE becomes even smaller as shown in Table 3.5 and Fig 3.5. Notice, that the XOR gates used are expanded as shown in the diagram.

3.3.1.3 TWO-BIT ADDER:

Fig. 3.6 shows the diagram for the 2-bit adder with 3 outputs. Six vectors were applied to this circuit. All XOR gates are primitive gates. However, HILO does not have an XOR primitive. Therefore, buffers must be placed at the inputs and output of each XOR gate. These buffers will prevent the simulator from injecting internal faults to the XOR gate. In other words, only input/output faults to XOR macro are considered.

However, for unknown reasons, HILO detects some faults at different steps. This may very well be due to some internal assumptions. In any case, if this problem is fixed, the MOE approaches zero. Table 3.6 shows these simulated results for the 2-bit adder. Table 3.7 shows the MOE calculations for all simulators and Table 3.8 shows these calculations without HILO. Figs. 3.7 and 3.8 are the plots for Tables 3.7 and 3.8 respectively. Again, the results are consistent and the simulators' fault coverage values tend to converge with the proposed calculation.




XOR

Fig. 3.3 8 Bits Binary To Gray Code Converter

( XOR expanded )

Table 3.3 GRAY CODE CONVERTER (XOR EXPANDED)

| Step | Number Faults Detected/step | | | | Number Classes Detected/step | | | |
|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS | HILO | LASAR | CADAT | HITS | HILO |
| 1 | 65 | 65 | 48 | 65 | 33 | 33 | 33 | 33 |
| 2 | 60 | 60 | 38 | 60 | 36 | 36 | 36 | 36 |
| 3 | 39 | 39 | 19 | 39 | 19 | 19 | 19 | 19 |
| 4 | 35 | 35 | 20 | 35 | 20 | 20 | 20 | 20 |

| Faults: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 199 | 199 | 125 | 199 |
| Potential Detections: | 0 | 0 | 0 | 0 |
| Undetectable: | 0 | 0 | 0 | 6* |
| Undetected: | 11 | 11 | 0 | 1 |
| Total: | 210 | 210 | 125 | 206** |

* HILO defines faults tied to GND or VCC as undetectable
** 4 faults are not listed by HILO

| Step | Cumulative Coverage (%) | | | | MOE (%) | Cumulative Standard Coverage | | | | MOE (%) |
|---|---|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS | HILO | | LASAR | CADAT | HITS | HILO | |
| 1 | 31.0 | 31.0 | 38.0 | 30.0 | 0.0-8.0 | 28.9 | 28.9 | 29.9 | 29.2 | 0.0-1.0 |
| 2 | 59.5 | 59.5 | 68.8 | 62.7 | 0.0-9.3 | 60.5 | 60.5 | 63.5 | 61.1 | 0.0-3.0 |
| 3 | 78.1 | 78.1 | 84.0 | 80.0 | 0.0-5.9 | 77.2 | 77.2 | 81.3 | 77.9 | 0.0-4.1 |
| 4 | 94.8 | 94.8 | 100. | 98.1 | 0.0-5.2 | 94.7 | 94.7 | 100. | 95.6 | 0.0-5.3 |

| Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 108 | 108 | 108 | 108 |
| Potential Detections: | 0 | 0 | 0 | 0 |
| Undetectable: | 0 | 0 | 0 | 4* |
| Undetected: | 6 | 6 | 0 | 1 |
| Total: | 114 | 114 | 108# | 113** |

MOE: Margin Of Error
* HILO defines faults tied to power supply as undetectable, however, for the purpose of comparison, these classes are considered as undetected.
** The GND SA/0 fault is not listed by HILO
# This is an optimistic # since ground faults were removed.

Table 3.4 GRAY CODE CONVERTER (XOR EXPANDED)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0-8.0 | 0.0-1.0 |
| 2 | 0.0-9.3 | 0.0-3.0 |
| 3 | 0.0-5.9 | 0.0-4.1 |
| 4 | 0.0-5.2 | 0.0-5.3 |

Margin Of Error before and after application of SFC

Table 3.5 GRAY CODE CONVERTER (XOR EXPANDED)
(HITS omitted in analysis)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0-1.0 | 0.0-0.3 |
| 2 | 0.0-3.2 | 0.0-0.6 |
| 3 | 0.0-1.9 | 0.0-0.7 |
| 4 | 0.0-3.3 | 0.0-0.9 |

Margin Of Error before and after application of SFC

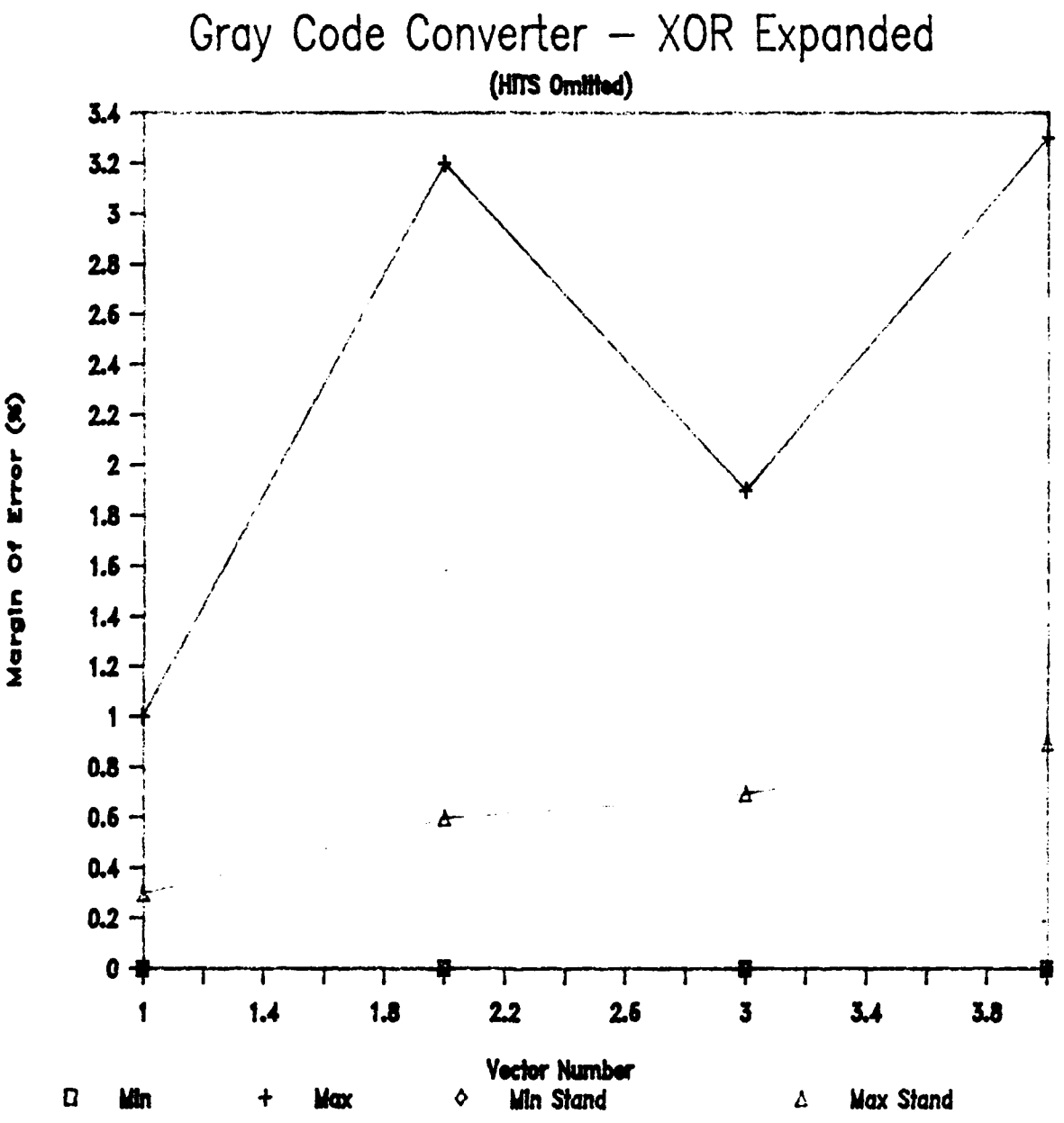

Gray Code Converter – XOR Expanded
(HITS Omitted)
Margin Of Error (%)
3.4
3.2
3
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
1
1.4
1.8
2.2
2.6
3
3.4
3.8
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.4

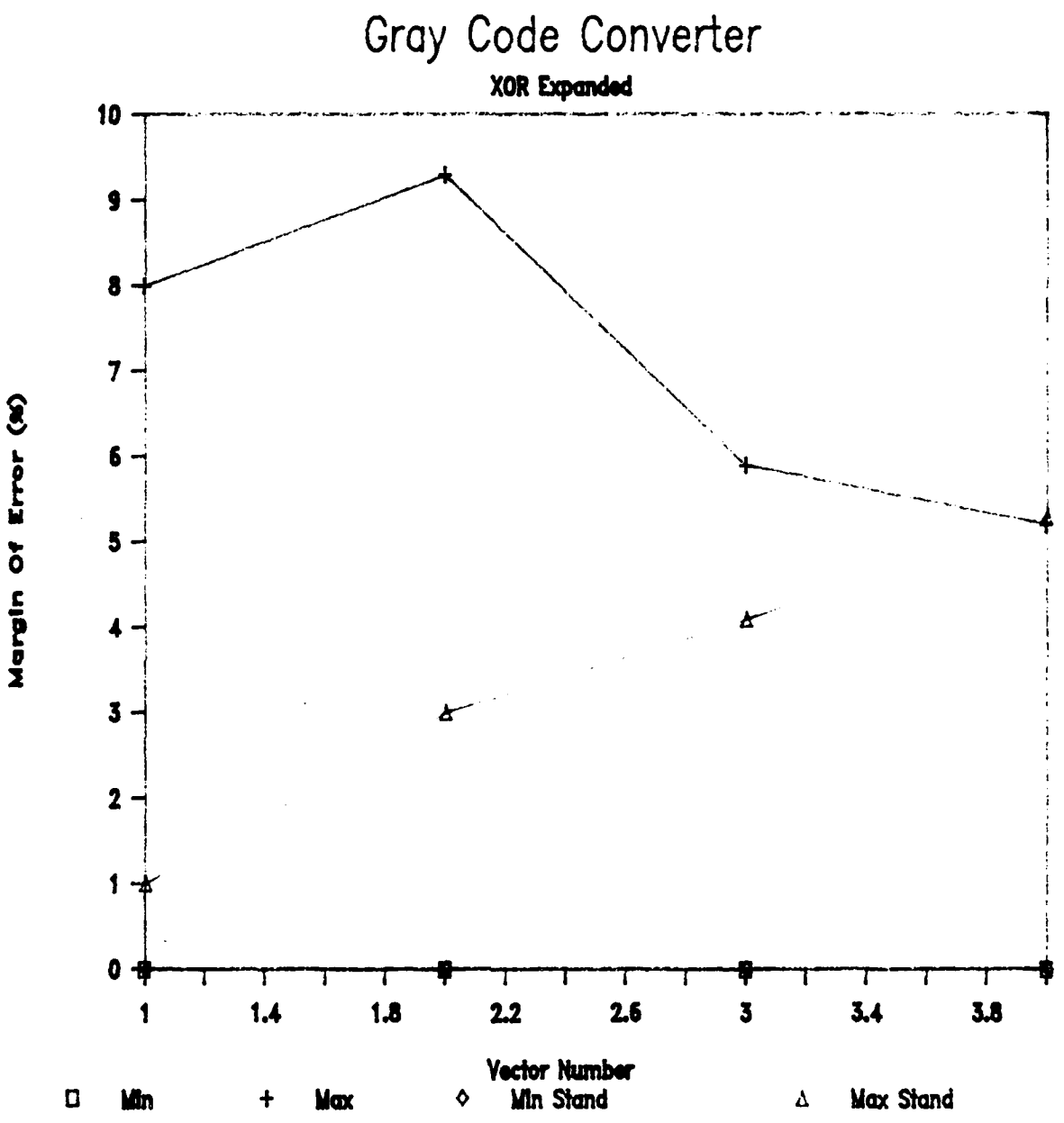

Gray Code Converter
XOR Expanded
Margin Of Error (%)
10
9
8
7
6
5
4
3
2
1
0
1
1.4
1.8
2.2
2.6
3
3.4
3.8
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.5

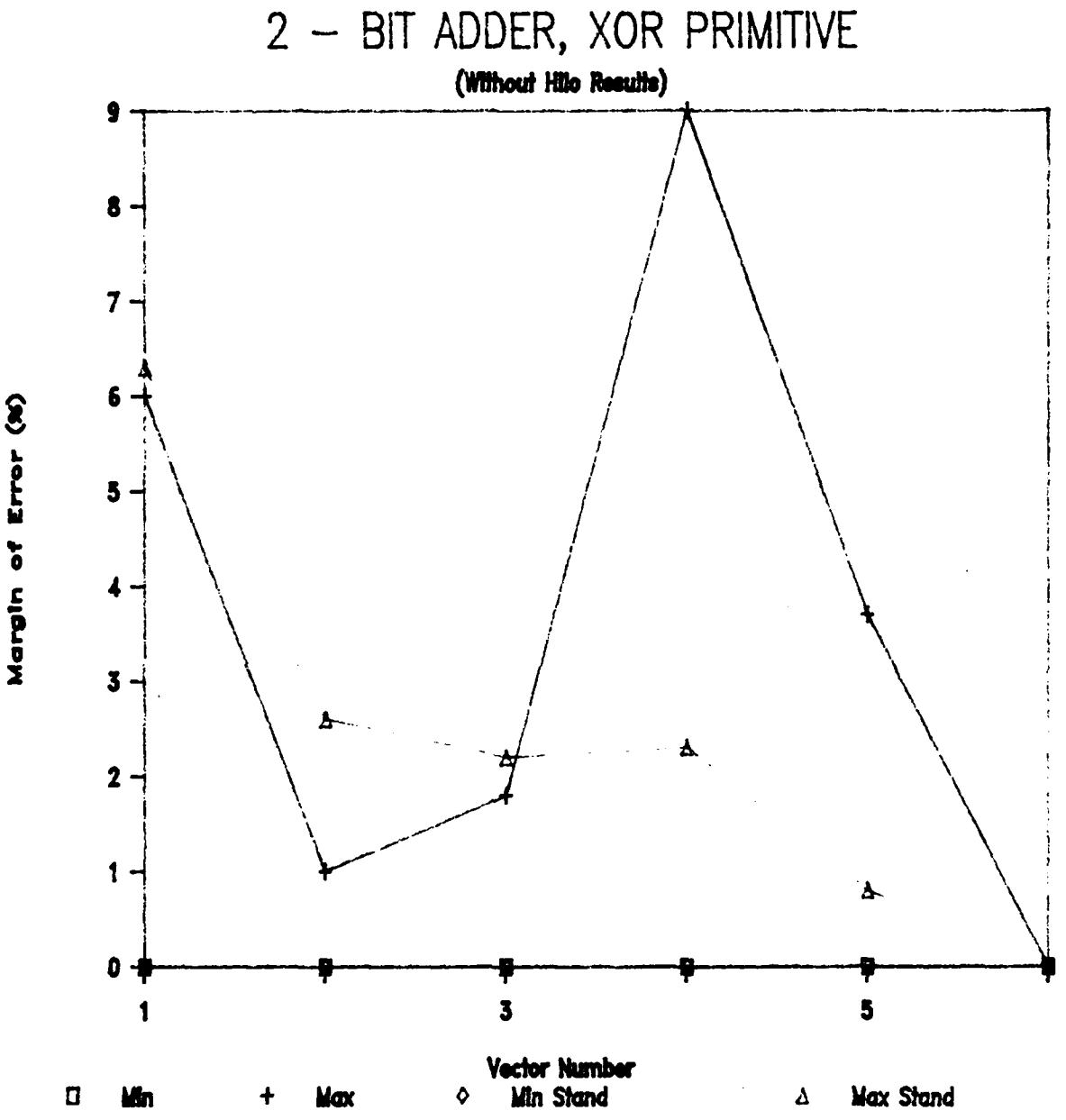

2 – BIT ADDER, XOR PRIMITIVE
(Without Hilo Results)
Margin of Error (%)
9
8
7
6
5
4
3
2
1
0
1
3
5
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.8

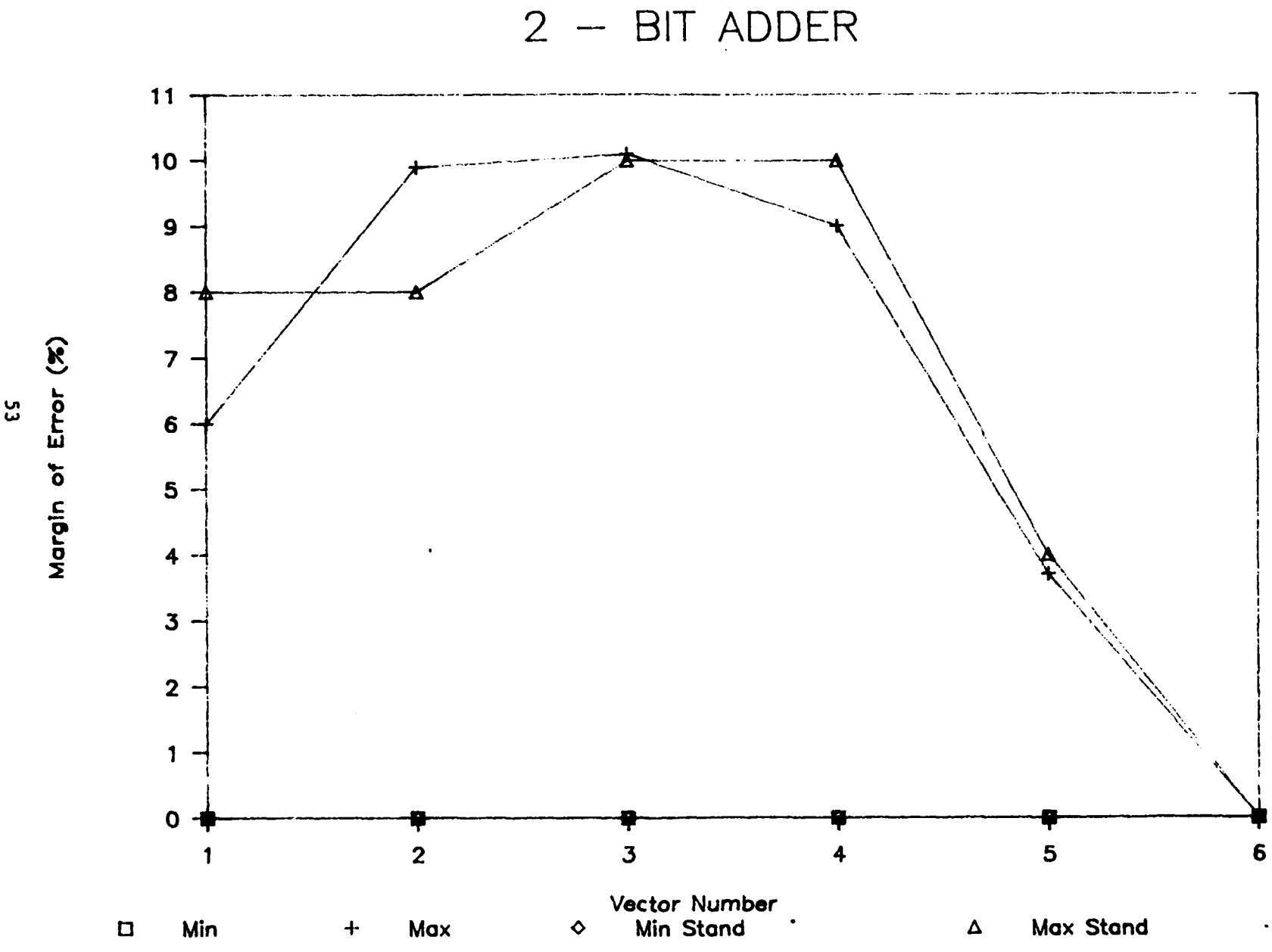

2 – BIT ADDER
Margin of Error (%)
11
10
9
8
7
6
5
4
3
2
1
0
1
2
3
4
5
6
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.7

Table 3.7 2 - BIT ADDER. XOR PRIMITIVE

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0- 6.0 | 0.0- 8.0 |
| 2 | 0.0- 9.9 | 0.0- 8.0 |
| 3 | 0.0-10.1 | 0.0-10.0 |
| 4 | 0.0- 9.0 | 0.0-10.0 |
| 5 | 0.0- 3.7 | 0.0- 4.0 |
| 6 | 0.0- 0.0 | 0.0- 0.0 |

Margin Of Error before and after application of SFC

Table 3.8 2 - BIT ADDER. XOR PRIMITIVE
WITHOUT HILO

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0- 6.0 | 0.0- 6.3 |
| 2 | 0.0- 1.0 | 0.0- 2.6 |
| 3 | 0.0- 1.7 | 0.0- 2.2 |
| 4 | 0.0- 9.0 | 0.0- 2.3 |
| 5 | 0.0- 3.7 | 0.0- 0.8 |
| 6 | 0.0- 0.0 | 0.0- 0.0 |

Margin Of Error before and after application of SFC

Table 3.6 2-BIT ADDER, XOR PRIMITIVE (VECTORS FROM HILO)

| Step | Number Faults Detected/step | | | | Number Classes Detected/step | | | | Cumulative Coverage (%) | | | | HOE | Cumulative Standard Coverage | | | | HOE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS | HILO | LASAR | CADAT | HITS | HILO | LASAR | CADAT | HITS | HILO | % | LASAR | CADAT | HITS | HILO | % |
| 1 | 27 | 27 | 15 | 23 | 21 | 21 | 15 | 17 | 38.6 | 38.6 | 32.6 | 34.0 | 0- 6.0 | 42.0 | 42.0 | 35.7 | 34.0 | 0- 8 |
| 2 | 24 | 24 | 19 | 23 | 16 | 16 | 15 | 15 | 72.9 | 72.9 | 73.9 | 64.0 | 0- 9.9 | 74.0 | 74.0 | 71.4 | 64.0 | 0-10 |
| 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 74.3 | 74.3 | 76.1 | 66.0 | 0-10.1 | 76.0 | 76.0 | 73.8 | 66.0 | 0-10 |
| 4 | 6 | 6 | 5 | 6 | 6 | 6 | 5 | 6 | 82.9 | 82.9 | 87.0 | 78.0 | 0- 9.0 | 88.0 | 88.0 | 85.7 | 78.0 | 0-10 |
| 5 | 7 | 7 | 4 | 10 | 4 | 4 | 4 | 7 | 92.9 | 92.9 | 95.7 | 92.0 | 0- 3.7 | 96.0 | 96.0 | 95.2 | 92.0 | 0- 4 |
| 6 | 5 | 5 | 2 | 7 | 2 | 2 | 2 | 4 | 100.0 | 100.0 | 100.0 | 100.0 | 0- 0.0 | 100.0 | 100.0 | 100.0 | 100.0 | 0- 0 |

| Faults: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 70 | 70 | 46 | 70 |
| Potential Detections: | 0 | 0 | 0 | 0 |
| Undetected: | 0 | 0 | 0 | 0 |
| Total: | 70 | 70 | 46 | 70* |

| Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 50 | 50 | 42 | 50 |
| Potential Detections: | 0 | 0 | 0 | 0 |
| Undetected: | 0 | 0 | 0 | 0 |
| Total: | 50 | 50 | 42 | 50* |

* HILO uses buffered XOR macro to inject the boundery faults

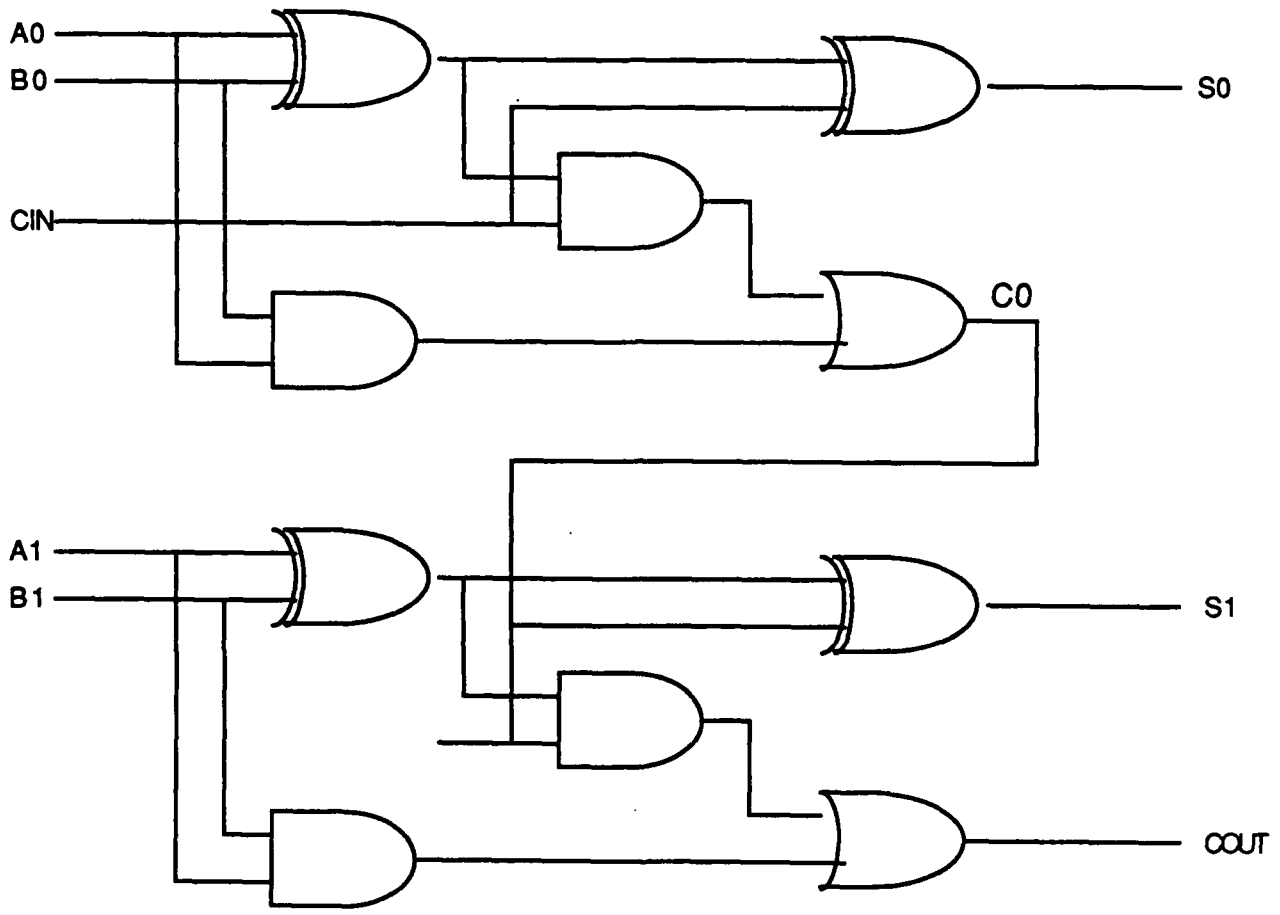



Fig. 3.6 Two - Bit Adder

3.3.1.4 FOUR-BIT COMPARATOR ( 74LS 85):

Fig. 3.9 shows the circuit diagram for the 4-bit comparator. A comparator circuit is of MSI complexity with many fanout points; eleven inputs and 3 outputs. The results of simulating such a circuit could be a good representative to similar circuits. The test vectors were provided by the government and Table 3.9 shows the simulated results. Again, the MOE while it is greater than zero when the simulators' fault coverages are compared, it is zero when all fault coverages are normalized to the standard calculation as shown in Table 3.10 and Fig. 3.10.

3.3.1.5 ALU (74LS181):

Fig. 3.11 shows the circuit diagram for the ALU with 14 inputs and 8 outputs. The A=B output is an open collector output. The fault at this node is handled differently by each simulator. For example HILO defines Open-Collector gate as weak 1, therefore, a fault at that node is solidly detected. On the other hand, CADAT and LASAR define detection at that node as potentially detected. HITS gives an optimistic value (same as Gray Code example) since it does not have potential detections.

In addition, two simulations were performed on this circuit, the first one is using all XOR gates as primitives as shown in Table 3.11. Again, HILO uses 16 macro cells for these gates. In this run, no buffers were used, and, hence, the number of faults are reduced by 32 and the number of classes are reduced by 16. Tables 3.13 and 3.14 and Figs. 3.12 and 3.13 show the MOE before and after the standard calculation which give the consistent findings. Table 3.12 shows the simulated results for the second run where all XOR gates were expanded. It is clear that the number of classes are almost the same with some differences which must be taken into consideration as recommended in chapter 4. CADAT has more classes due to the fact that any primary input with no fanout (subsection 2.2.1.1, ex. 5)

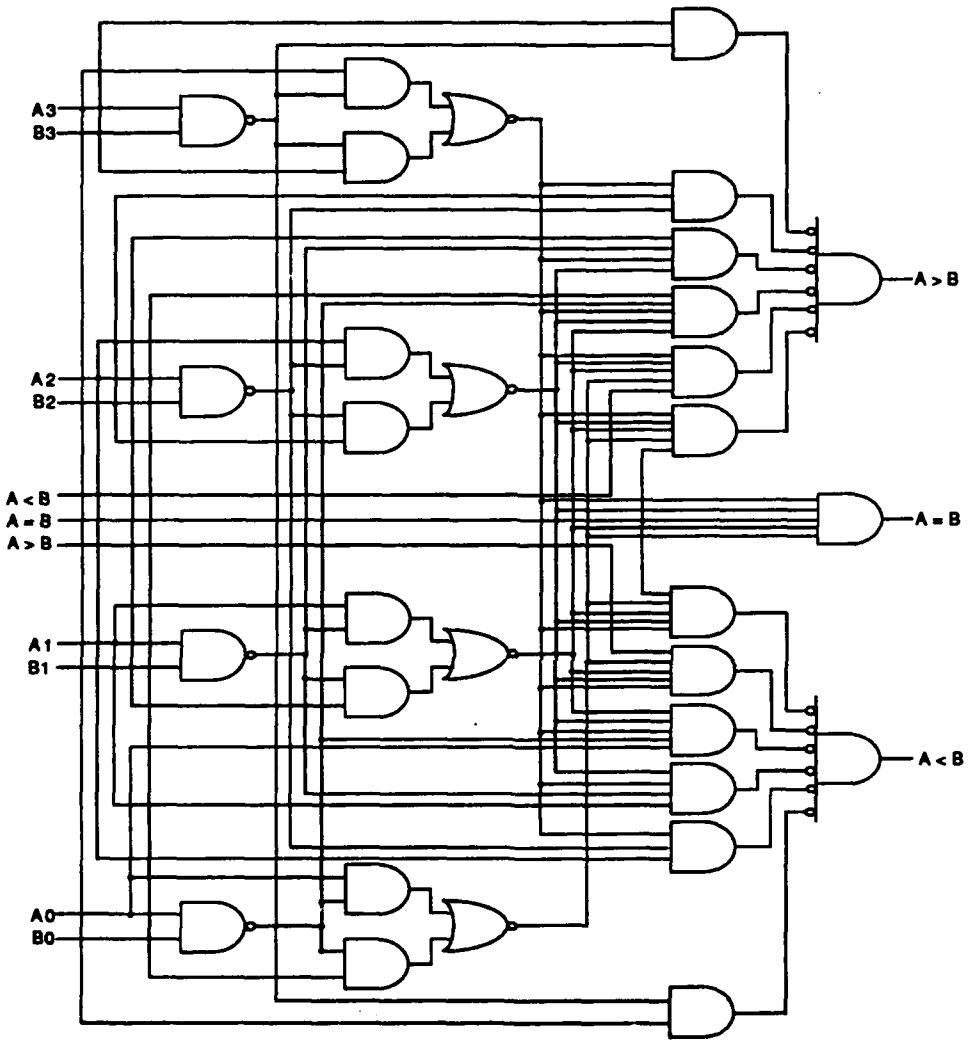



**Figure 3.9. 7485 Comparator circuit**

# TABLE 3.9

4-BIT COMPARATOR 85 (VECTORS FROM AF)

| Step | Number Faults Detected/step | | | | Number Classes Detected/step | | | | Cumulative Coverage (%) | | | | | Cumulative Standard Coverage | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS | HILO | LASAR | CADAT | HITS | HILO | LASAR | CADAT | HITS | HILO | MOE | LASAR | CADAT | HITS | HILO | MOE |
| 1 | 76 | 76 | 47 | 76 | 32 | 34 | 32 | 32 | 27.3 | 27.3 | 29.6 | 23.3 | 0.0-6.3 | 23.3 | 23.3 | 23.3 | 23.3 | 0.0-0.0 |
| 2 | 46 | 46 | 31 | 46 | 25 | 25 | 25 | 25 | 43.9 | 43.9 | 49.1 | 41.6 | 0.0-7.5 | 41.6 | 41.6 | 41.6 | 41.6 | 0.0-0.0 |
| 3 | 22 | 22 | 14 | 22 | 14 | 14 | 14 | 14 | 51.8 | 51.8 | 57.9 | 51.8 | 0.0-6.1 | 51.8 | 51.8 | 51.8 | 51.8 | 0.0-0.0 |
| 4 | 19 | 19 | 12 | 19 | 11 | 13 | 11 | 11 | 58.6 | 58.6 | 65.4 | 59.8 | 0.0-6.8 | 59.8 | 59.8 | 59.8 | 59.8 | 0.0-0.0 |
| 5 | 15 | 15 | 8 | 15 | 8 | 8 | 8 | 8 | 64.0 | 64.0 | 70.4 | 65.6 | 0.0-6.4 | 65.6 | 65.6 | 65.6 | 65.6 | 0.0-0.0 |
| 6 | 14 | 14 | 8 | 14 | 8 | 8 | 8 | 8 | 69.1 | 69.1 | 75.5 | 71.5 | 0.0-6.4 | 71.5 | 71.5 | 71.5 | 71.5 | 0.0-0.0 |
| 7 | 16 | 16 | 7 | 16 | 7 | 7 | 7 | 7 | 74.8 | 74.8 | 79.9 | 76.6 | 0.0-5.1 | 76.6 | 76.6 | 76.6 | 76.6 | 0.0-0.0 |
| 8 | 13 | 13 | 5 | 13 | 5 | 5 | 5 | 5 | 79.5 | 79.5 | 83.0 | 80.2 | 0.0-3.5 | 80.2 | 80.2 | 80.2 | 80.2 | 0.0-0.0 |
| 9 | 12 | 12 | 5 | 12 | 5 | 5 | 5 | 5 | 83.8 | 83.8 | 86.1 | 83.9 | 0.0-2.3 | 83.9 | 83.9 | 83.9 | 83.9 | 0.0-0.0 |
| 10 | 11 | 11 | 5 | 11 | 5 | 5 | 5 | 5 | 87.8 | 87.8 | 89.3 | 87.5 | 0.0-1.8 | 87.5 | 87.5 | 87.5 | 87.5 | 0.0-0.0 |
| 11 | 21 | 21 | 4 | 21 | 4 | 4 | 4 | 4 | 95.3 | 95.3 | 91.8 | 90.5 | 0.0-4.8 | 90.5 | 90.5 | 90.5 | 90.5 | 0.0-0.0 |
| 12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 95.7 | 95.7 | 92.5 | 91.2 | 0.0-4.5 | 91.2 | 91.2 | 91.2 | 91.2 | 0.0-0.0 |
| 13 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 96.0 | 96.0 | 93.1 | 91.9 | 0.0-4.1 | 91.9 | 91.9 | 91.9 | 91.9 | 0.0-0.0 |
| 14 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 96.4 | 96.4 | 93.7 | 92.7 | 0.0-3.7 | 92.7 | 92.7 | 92.7 | 92.7 | 0.0-0.0 |
| 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 96.8 | 96.8 | 94.3 | 93.4 | 0.0-3.4 | 93.4 | 93.4 | 93.4 | 93.4 | 0.0-0.0 |
| 16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 97.1 | 97.1 | 95.0 | 94.1 | 0.0-3.0 | 94.1 | 94.1 | 94.1 | 94.1 | 0.0-0.0 |
| 17 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 97.5 | 97.5 | 95.6 | 94.8 | 0.0-2.7 | 94.8 | 94.8 | 94.8 | 94.8 | 0.0-0.0 |
| 18 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 97.8 | 97.8 | 96.2 | 95.6 | 0.0-2.2 | 95.6 | 95.6 | 95.6 | 95.6 | 0.0-0.0 |
| 19 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 98.2 | 98.2 | 96.9 | 96.3 | 0.0-1.9 | 96.3 | 96.3 | 96.3 | 96.3 | 0.0-0.0 |
| 20 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 98.6 | 98.6 | 97.5 | 97.0 | 0.0-1.6 | 97.0 | 97.0 | 97.0 | 97.0 | 0.0-0.0 |
| 21 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 98.9 | 98.9 | 98.1 | 97.8 | 0.0-1.1 | 97.8 | 97.8 | 97.8 | 97.8 | 0.0-0.0 |
| 22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 99.3 | 99.3 | 98.7 | 98.5 | 0.0-0.8 | 98.5 | 98.5 | 98.5 | 98.5 | 0.0-0.0 |
| 23 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 99.6 | 99.6 | 99.4 | 99.2 | 0.0-0.2 | 99.2 | 99.2 | 99.2 | 99.2 | 0.0-0.0 |
| 24 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 100.0 | 100.0 | 100.0 | 100.0 | 0-0 | 100.0 | 100.0 | 100.0 | 100.0 | 0.0-0.0 |

| Faults: | LASAR | CADAT | HITS | HILO | Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|---|---|---|---|---|
| Solid Detections: | 278 | 278 | 159 | 278 | Solid Detections: | 137 | 141 | 137 | 137 |
| Potential Detections: | 0 | 0 | 0 | 0 | Potential Detections: | 0 | 0 | 0 | 0 |
| Undetected: | 0 | 0 | 0 | 0 | Undetected: | 0 | 0 | 0 | 0 |
| Total: | 278 | 278 | 159 | 278 | Total: | 137 | 141 | 137 | 137 |

Table 3.10. 4-bit Comparator 7485 (vectors from AF)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0-6.3 | 0.0-0.0 |
| 2 | 0.0-7.5 | 0.0-0.0 |
| 3 | 0.0-6.1 | 0.0-0.0 |
| 4 | 0.0-6.8 | 0.0-0.0 |
| 5 | 0.0-6.4 | 0.0-0.0 |
| 6 | 0.0-6.4 | 0.0-0.0 |
| 7 | 0.0-5.1 | 0.0-0.0 |
| 8 | 0.0-3.5 | 0.0-0.0 |
| 9 | 0.0-2.3 | 0.0-0.0 |
| 10 | 0.0-1.8 | 0.0-0.0 |
| 11 | 0.0-4.8 | 0.0-0.0 |
| 12 | 0.0-4.5 | 0.0-0.0 |
| 13 | 0.0-4.1 | 0.0-0.0 |
| 14 | 0.0-3.7 | 0.0-0.0 |
| 15 | 0.0-3.4 | 0.0-0.0 |
| 16 | 0.0-3.0 | 0.0-0.0 |
| 17 | 0.0-2.7 | 0.0-0.0 |
| 18 | 0.0-2.2 | 0.0-0.0 |
| 19 | 0.0-1.9 | 0.0-0.0 |
| 20 | 0.0-1.6 | 0.0-0.0 |
| 21 | 0.0-1.1 | 0.0-0.0 |
| 22 | 0.0-0.8 | 0.0-0.0 |
| 23 | 0.0-0.2 | 0.0-0.0 |
| 24 | 0.0-0.0 | 0.0-0.0 |

Margin Of Error before and after application of SFC

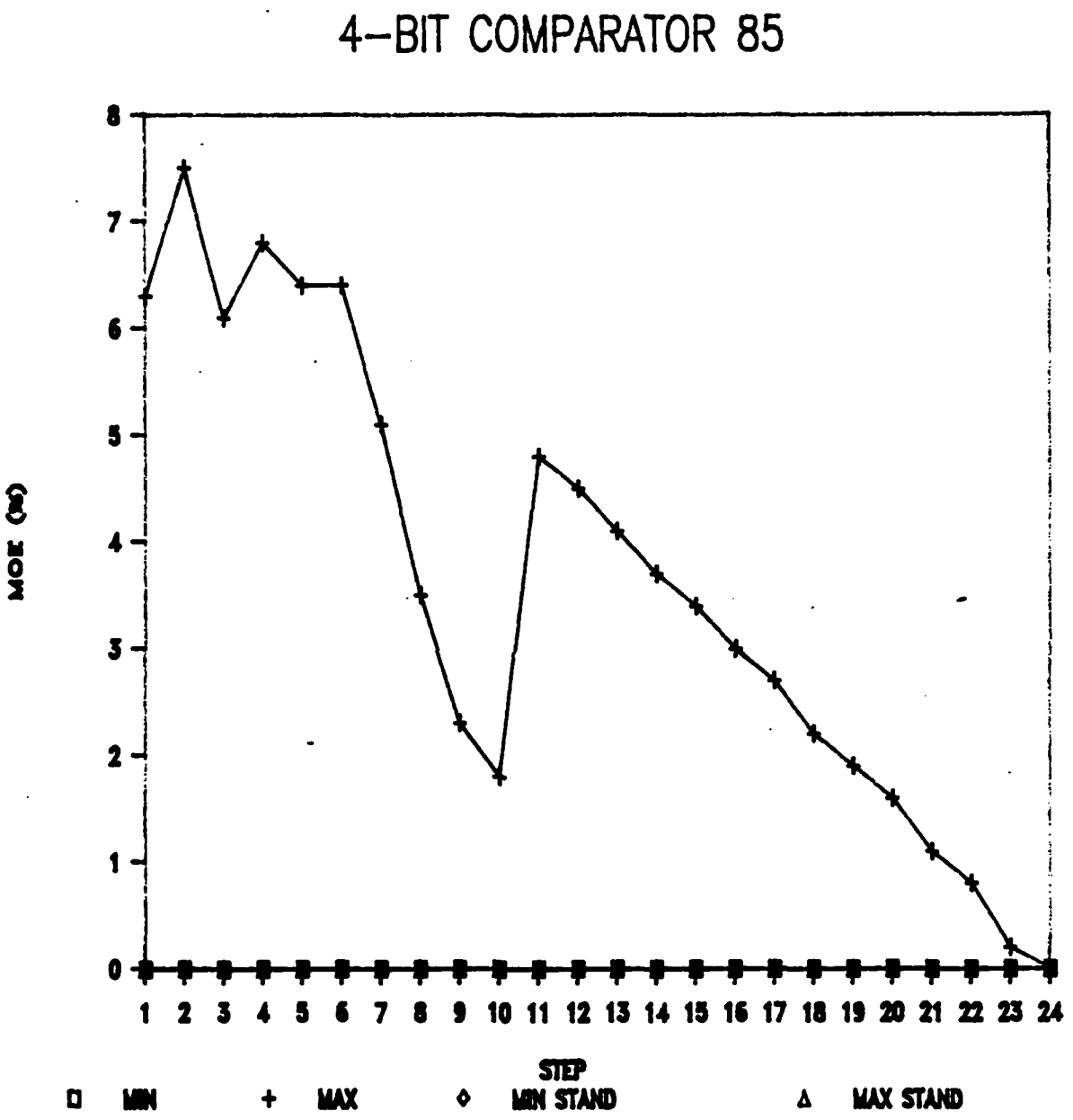

4-BIT COMPARATOR 85
MOE (%)
0
1
2
3
4
5
6
7
8
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
STEP
MIN
MAX
MIN STAND
MAX STAND

Fig. 3.10

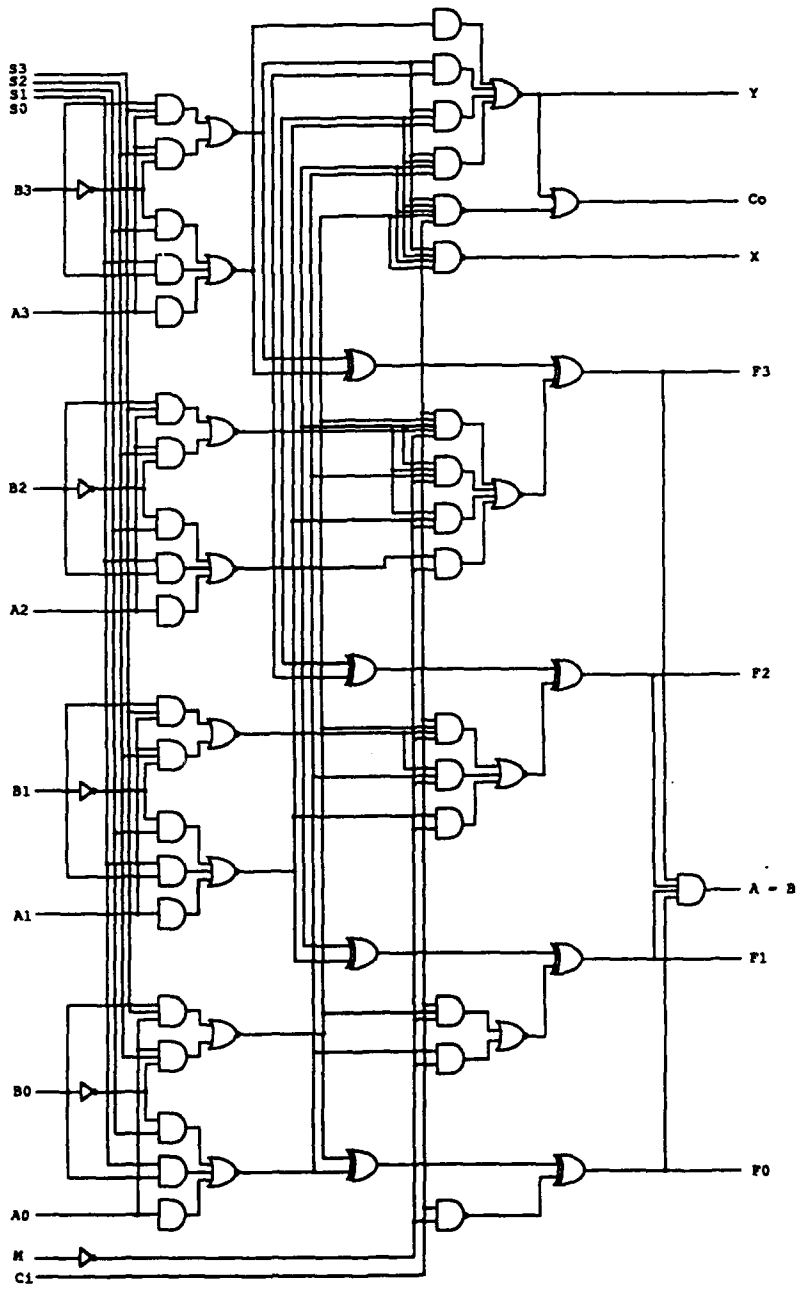



**Figure 3.11. ALU 74181 circuit**

## TABLE 3.11

ALU 181 - XOR AS PRIMITIVES

| Step | Number Faults Detected/step LASAR | CADAT | HITS | HILO | Number Classes Detected/step LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|---|---|---|---|
| 1 | 140-2 | 140 | 107 | 125 | 70-71 | 73 | 96 | 62 |
| 2 | 83-84 | 83-84 | 69 | 74 | 48-49 | 51-52 | 63 | 44 |
| 3 | 54-55 | 54-55 | 37 | 51 | 28-29 | 29-30 | 32 | 27 |
| 4 | 56 | 56 | 22 | 60 | 17 | 17 | 16 | 18 |
| 5 | 29 | 29 | 18 | 28 | 15 | 15 | 14 | 14 |
| 6 | 16 | 16 | 13 | 16 | 13 | 13 | 13 | 13 |
| 7 | 20-21 | 20-21 | 10 | 21 | 9-10 | 9-10 | 10 | 10 |
| 8 | 10 | 10 | 7 | 10 | 7 | 7 | 7 | 7 |
| 9 | 5-6 | 5-6 | 6 | 6 | 2 | 5-6 | 6 | 6 |
| 10 | 16 | 16 | 3 | 16 | 2 | 3 | 3 | 3 |
| 11 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 12 | 10 | 10 | 2 | 10 | 2-3 | 2 | 2 | 2 |
| 13 | 4 | 4 | 1 | 4 | 1 | 1 | 1 | 1 |
| 14 | 5 | 5 | 1 | 5 | 1 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Faults: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 451 | 451 | 299 | 428 |
| Potential Detections: | 6 | 4 | 0 | 0* |
| Undetected: | 7 | 5 | 0 | 0 |
| Total: | 464 | 460 | 299 | 428** |

* HILO defines the OC gate as WEAK 1 with no potencial faults
** HILO uses 8 unbuffered micro XORs and 32 boundary faults on these micros are missing

ALU 181 - XOR AS PRIMITIVES

| Step | Cumulative Coverage (%) LASAR | CADAT | HITS | HILO | MOE (%) | Cumulative Standard Coverage LASAR | CADAT | HITS | HILO | MOE (%) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 30.2-0.4 | 30.4 | 35.8 | 29.3 | 0.2-5.6 | 30.8-31.3 | 31.0 | 39.5 | 29.3 | 0.8-8.7 |
| 2 | 48.1-0.6 | 48.5-48.7 | 58.9 | 50.2 | .4-10.8 | 52.0-52.9 | 53.0-53.4 | 59.5 | 50.2 | 1.0-9.3 |
| 3 | 59.7-0.9 | 60.2-60.7 | 71.2 | 63.0 | .5-11.5 | 64.3-65.6 | 65.1-65.9 | 71.5 | 63.0 | 0.8-8.5 |
| 4 | 71.8 | 72.4-72.8 | 78.6 | 71.5 | 0.3-7.1 | 71.8-73.1 | 72.4-73.3 | 77.5 | 71.5 | 0.3-6.0 |
| 5 | 78.0 | 78.7-79.1 | 84.6 | 78.1 | 0.1-6.6 | 78.4-79.7 | 78.9-79.7 | 82.7 | 78.1 | 0.3-4.6 |
| 6 | 81.5 | 82.2-82.6 | 89.0 | 84.3 | 0.7-7.5 | 84.1-85.5 | 84.5-85.3 | 87.6 | 84.3 | 0.2-3.5 |
| 7 | 85.8-1.1 | 86.5-87.2 | 92.3 | 89.0 | 0.8-6.5 | 88.1-89.9 | 88.4-89.7 | 91.3 | 89.0 | 0.3-3.3 |
| 8 | 87.9 | 88.7-89.4 | 94.7 | 92.4 | 0.8-6.8 | 91.2-93.0 | 91.4-92.7 | 94.0 | 92.4 | 0.2-2.8 |
| 9 | 89.0-1.3 | 89.8-90.7 | 96.7 | 95.2 | 0.8-7.7 | 92.1-93.8 | 93.5-95.3 | 96.2 | 95.2 | 1.0-4.1 |
| 10 | 92.5 | 93.3-94.1 | 97.7 | 96.6 | 0.8-5.2 | 93.0-94.7 | 94.8-96.6 | 97.3 | 96.6 | 0.7-4.3 |
| 11 | 92.9 | 93.7-94.6 | 98.3 | 97.6 | 0.8-5.4 | 93.8-95.6 | 95.7-97.4 | 98.1 | 97.6 | 0.5-4.3 |
| 12 | 95.0 | 95.9-96.7 | 99.0 | 98.5 | 0.9-4.0 | 95.2-96.9 | 96.6-98.3 | 98.8 | 98.5 | 0.3-3.6 |
| 13 | 95.9 | 96.7-97.6 | 99.3 | 99.0 | 0.8-3.4 | 95.6-97.4 | 97.0-98.7 | 99.2 | 99.0 | 0.2-3.6 |
| 14 | 97.0 | 97.8-98.7 | 99.7 | 99.5 | 0.8-2.7 | 96.0-97.8 | 97.4-99.1 | 99.6 | 99.5 | 0.1-3.6 |
| 15 | 97.2-1.3 | 98.0-98.9 | 100. | 100. | 0.8-2.8 | 96.4-98.2 | 97.8-99.6 | 100. | 100. | 0-3.6 |

| Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 222 | 229 | 267# | 211 |
| Potential Detections: | 5 | 4 | 0 | 0* |
| Undetected: | 1 | 1 | 0 | 0 |
| Total: | 228 | 234 | 267 | 211** |

MOE: Margin Of Error
* HILO defines OC gate as WEAK 1 and no potencial faults on OC gate
** HILO uses 16 unbuffered micro XORs and 16 fault classes on the boundary of these micros are missing .
\# extra fault classes are added due to boundary faults at each macro PO.

## TABLE 3.12

ALU 181 - XOR EXPANDED

| Step | Number Faults Detected/step LASAR | CADAT | HITS | HILO | Number Classes Detected/step LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|---|---|---|---|
| 1 | 178-80 | 184 | 133 | 184 | 77 | 77 | 76 | 76 |
| 2 | 119-20 | 125-26 | 91 | 126 | 58 | 60-61 | 56 | 56 |
| 3 | 74-75 | 78-79 | 51 | 79 | 35 | 35-36 | 36 | 36 |
| 4 | 71 | 73 | 31 | 78 | 20 | 20 | 19 | 21 |
| 5 | 36 | 38 | 23 | 38 | 20 | 20 | 19 | 20 |
| 6 | 16 | 16 | 13 | 16 | 13 | 13 | 13 | 13 |
| 7 | 20-21 | 20-21 | 10 | 21 | 10 | 9-10 | 10 | 10 |
| 8 | 10 | 10 | 7 | 10 | 7 | 7 | 7 | 7 |
| 9 | 5-6 | 5-6 | 6 | 6 | 5-6 | 5-6 | 6 | 6 |
| 10 | 16 | 16 | 3 | 16 | 3 | 3 | 3 | 3 |
| 11 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| 12 | 10 | 10 | 2 | 10 | 2 | 2 | 2 | 2 |
| 13 | 4 | 4 | 1 | 4 | 1 | 1 | 1 | 1 |
| 14 | 5 | 5 | 1 | 5 | 1 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| Faults: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 567 | 587 | 375 | 596 |
| Potential Detections: | 6 | 4 | 0 | 0* |
| Undetected: | 31 | 29 | 12 | 24 |
| Total: | 604 | 620 | 387 | 620 |

* HILO defines OC gate as WEAK 1 with no potencial faults

ALU 181 - XOR EXPANDED

| Step | Cumulative Coverage (%) LASAR | CADAT | HITS | HILO | MOE (%) | Cumulative Standard Coverage LASAR | CADAT | HITS | HILO | MOE (%) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 29.5-.3 | 29.7 | 34.4 | 29.3 | 0.2-4.9 | 29.6 | 28.8 | 29.6 | 29.3 | 0-0.8 |
| 2 | 49.2-.5 | 49.8-50.0 | 57.9 | 50.9 | 0.6-8.7 | 51.9 | 51.1-58.6 | 51.5 | 50.9 | 0.4-7.7 |
| 3 | 61.4-.7 | 62.4-62.7 | 71.1 | 64.8 | 1.0-9.7 | 65.4 | 64.4-65.2 | 65.6 | 64.8 | 0.2-1.2 |
| 4 | 73.2-.7 | 74.2-74.5 | 79.1 | 72.9 | 0.3-6.2 | 73.1 | 72.0-72.7 | 73.0 | 72.9 | 0.1-1.1 |
| 5 | 79.1-.7 | 80.3-80.7 | 85.0 | 80.6 | 0.3-5.9 | 80.8 | 79.5-80.3 | 80.4 | 80.6 | 0.2-1.3 |
| 6 | 81.8-.7 | 82.9-83.2 | 88.4 | 85.7 | 1.1-6.6 | 85.8 | 84.5-85.2 | 85.5 | 85.7 | 0.2-1.3 |
| 7 | 85.1-.8 | 86.1-86.6 | 91.0 | 89.5 | 0.5-5.9 | 89.6 | 87.9-89.0 | 89.4 | 89.5 | 0.1-1.7 |
| 8 | 86.8-.8 | 87.7-88.2 | 92.8 | 92.2 | 0.6-6.0 | 92.3 | 90.5-91.7 | 92.1 | 92.2 | 0.1-1.8 |
| 9 | 87.6- 1 | 88.6-89.2 | 94.3 | 94.5 | 0.2-6.9 | 94.2-94.6 | 92.4-93.9 | 94.5 | 94.5 | 0-2.2 |
| 10 | 90.2- 1 | 91.1-91.8 | 95.1 | 95.7 | 0.5-5.5 | 95.4-95.8 | 93.5-95.1 | 95.7 | 95.7 | 0-2.3 |
| 11 | 90.6- 1 | 91.5-92.1 | 95.6 | 96.5 | 0.9-5.9 | 96.2-96.5 | 94.3-95.8 | 96.4 | 96.5 | 0.1-2.2 |
| 12 | 92.2- 1 | 93.1-93.7 | 96.1 | 97.2 | 0.9-5.0 | 96.9-97.3 | 95.1-96.6 | 97.2 | 97.2 | 0-2.2 |
| 13 | 92.9- 1 | 93.7-94.4 | 96.4 | 97.6 | 0.8-4.8 | 97.3-97.7 | 95.5-97.0 | 97.6 | 97.6 | 0-2.2 |
| 14 | 93.7- 1 | 94.5-95.2 | 96.6 | 98.0 | 0.8-4.3 | 97.7-98.1 | 95.8-97.3 | 98.0 | 98.0 | 0-2.3 |
| 15 | 93.9- 1 | 94.7-95.3 | 96.8 | 98.4 | 0.8-4.5 | 98.1-98.5 | 96.2-97.7 | 98.4 | 98.4 | 0-2.3 |

| Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 251 | 256 | 252 | 255 |
| Potential Detections: | 4 | 4 | 0 | 0* |
| Undetected: | 5 | 6 | 4 | 4 |
| Total: | 260 | 266 | 256 | 259 |

MOE: Margin Of Error
* HILO defines OC gate as WEAK 1 and no potencial faults on OC gate

Table 3.13. ALU 74181 - Xor as primitives

(Solid + potential detections)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.2- 5.6 | 0.3-8.7 |
| 2 | 0.0-10.2 | 0.5-9.3 |
| 3 | 0.1-10.6 | 0.3-8.5 |
| 4 | 0.3- 7.1 | 0.2-6.0 |
| 5 | 0.1- 6.6 | 0.0-4.6 |
| 6 | 1.1- 7.5 | 0.2-3.5 |
| 7 | 0.3- 5.4 | 0.2-3.3 |
| 8 | 1.5- 6.8 | 0.3-2.8 |
| 9 | 0.4- 6.4 | 1.0-2.4 |
| 10 | 1.1- 5.2 | 0.0-2.6 |
| 11 | 0.7- 5.4 | 0.2-2.5 |
| 12 | 1.5- 4.0 | 0.2-1.9 |
| 13 | 0.3- 3.4 | 0.2-2.2 |
| 14 | 0.2- 2.7 | 0.1-1.8 |
| 15 | 0.0- 2.5 | 0.0-1.8 |

Margin Of Error before and after application of SFC

Table 3.14. ALU 74181 - Xor as primitives
(Solid detections only)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.2- 5.6 | 0.8-8.7 |
| 2 | 0.4-10.8 | 1.0-9.3 |
| 3 | 0.5-11.5 | 0.8-8.5 |
| 4 | 0.3- 7.1 | 0.3-6.0 |
| 5 | 0.1- 6.6 | 0.3-4.6 |
| 6 | 0.7- 7.5 | 0.2-3.5 |
| 7 | 0.7- 6.5 | 0.3-3.3 |
| 8 | 0.8- 6.8 | 0.2-2.8 |
| 9 | 0.8- 7.7 | 1.0-4.1 |
| 10 | 0.8- 5.2 | 0.7-4.3 |
| 11 | 0.8- 5.4 | 0.5-4.3 |
| 12 | 0.9- 4.0 | 0.3-3.6 |
| 13 | 0.8- 3.4 | 0.2-3.6 |
| 14 | 0.8- 2.7 | 0.1-3.6 |
| 15 | 0.8- 2.8 | 0.0-3.6 |

Margin Of Error before and after application of SFC

Table 3.15. ALU 74181 - Xor expanded
(vectors from AF)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.2-4.9 | 0.0-0.8 |
| 2 | 0.6-8.7 | 0.2-7.7 |
| 3 | 1.0-9.7 | 0.2-1.2 |
| 4 | 0.3-6.2 | 0.1-1.1 |
| 5 | 0.3-5.9 | 0.2-1.3 |
| 6 | 1.1-6.6 | 0.2-1.3 |
| 7 | 0.5-5.9 | 0.1-1.7 |
| 8 | 0.6-6.0 | 0.1-1.8 |
| 9 | 0.2-6.9 | 0.0-2.2 |
| 10 | 0.6-5.5 | 0.0-2.3 |
| 11 | 0.9-5.9 | 0.1-2.2 |
| 12 | 0.9-5.0 | 0.0-2.2 |
| 13 | 0.8-4.8 | 0.0-2.2 |
| 14 | 0.8-4.3 | 0.0-2.3 |
| 15 | 0.8-4.5 | 0.0-2.3 |

Margin Of Error before and after application of SFC

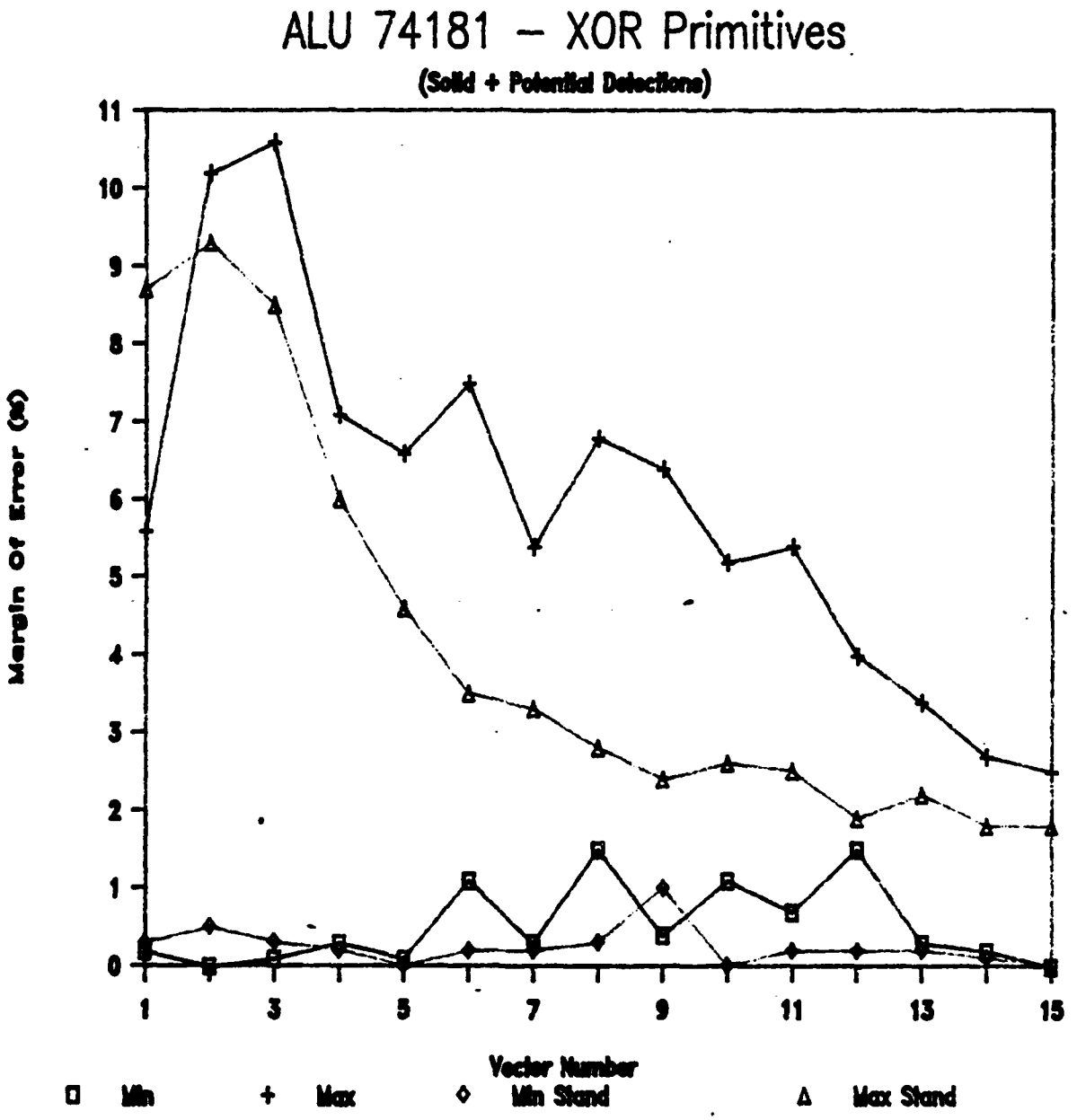

ALU 74181 – XOR Primitives
(Solid + Potential Detections)
Margin Of Error (%)
11
10
9
8
7
6
5
4
3
2
1
0
1
3
5
7
9
11
13
15
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.12

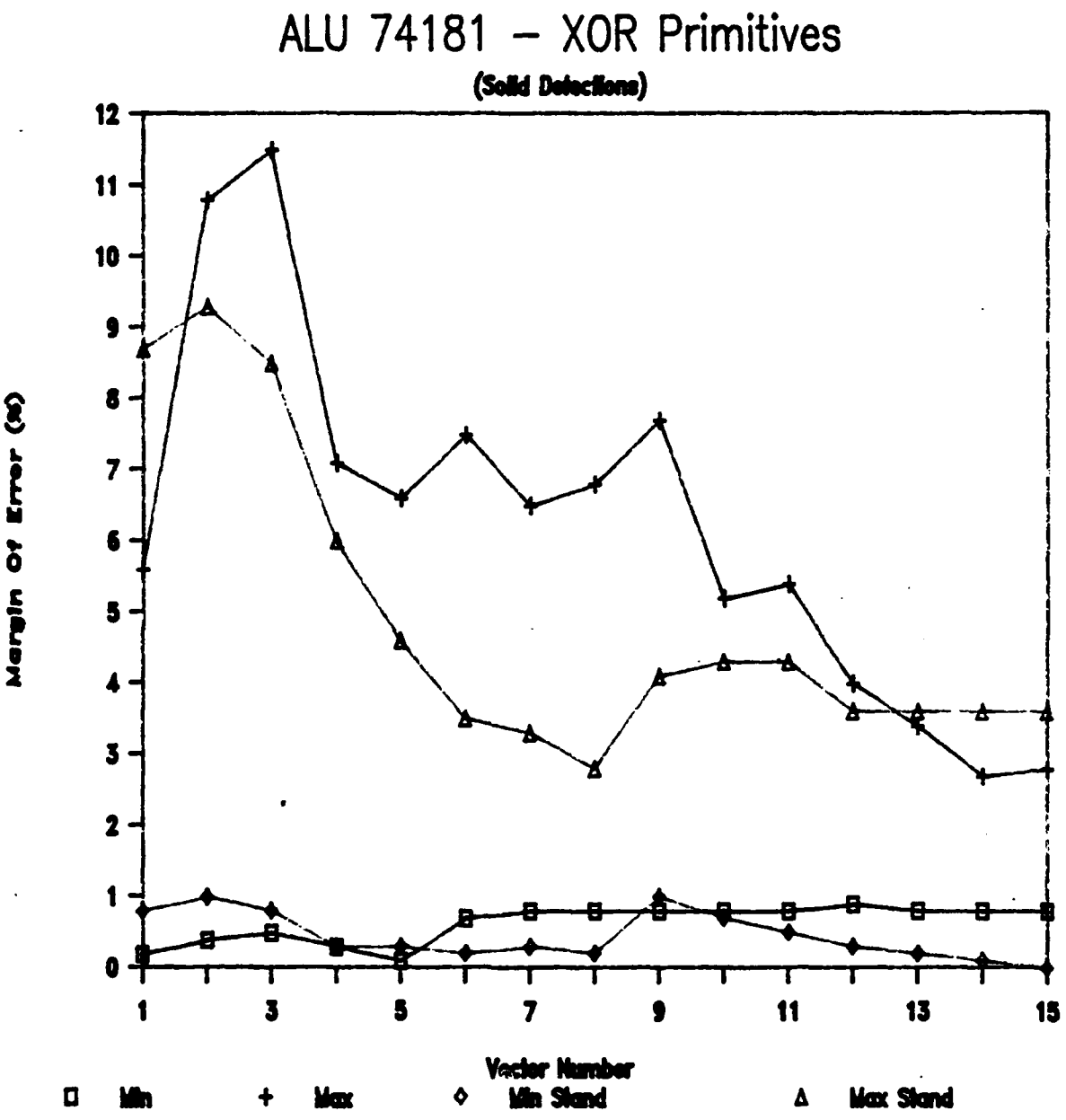

ALU 74181 – XOR Primitives
(Solid Detections)
Margin Of Error (%)
12
11
10
9
8
7
6
5
4
3
2
1
0
1
3
5
7
9
11
13
15
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.13

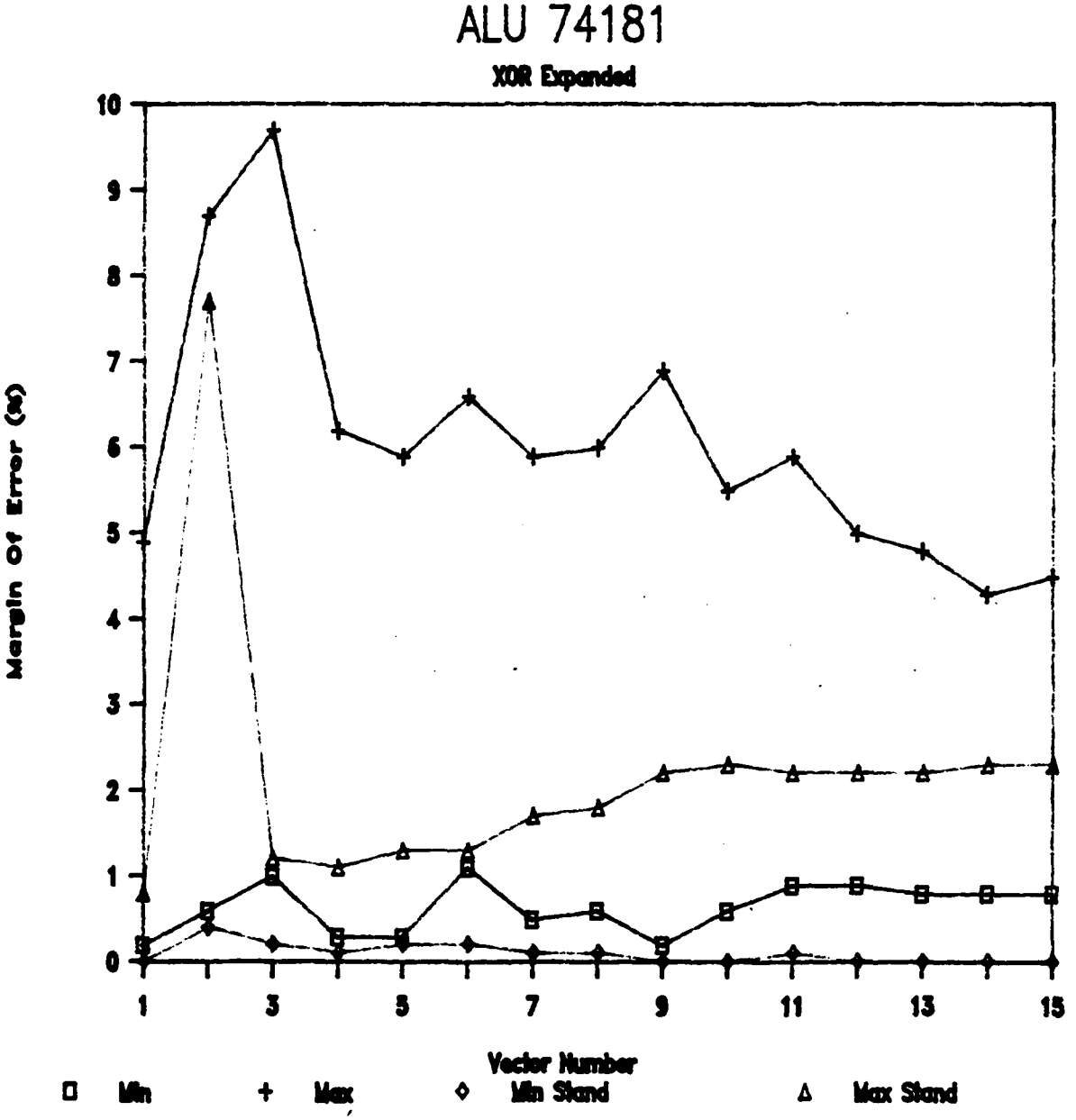

ALU 74181
XOR Expanded
Margin Of Error (%)
10
9
8
7
6
5
4
3
2
1
0
1
3
5
7
9
11
13
15
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.14

is classified in a separate class from the fault class at the input of the gate. All other simulators will have these two classes collapse to a single class. Table 3.15 and Fig. 3.14 show the results for the ALU with expanded XOR where the fault coverages of the simulators are converging when using the standard calculation.

### 3.3.2 SEQUENTIAL CIRCUITS:

Several circuits with sequential elements were simulated where faults were injected and the fault coverage evaluated. Here, we also applied the same rules and the new fault coverage evaluation was also compared to the given one. It must be noted, however, that LASAR and HILO had to be sometimes taken from some of the evaluations, due to the fact that different faults were being injected. These cases will be pointed out and explained. In addition, some inconsistent results were obtained and after analyzing them it is believed that these inconsistencies are a function of the simulator and not the circuit. These also will be pointed out in the discussion when they come up. The following is the result of the simulation of the sequential circuits.

#### 3.3.2.1 EDGE-TRIGGERED DELAY FLIP-FLOP

Fig. 3.15 shows the circuit diagram of the edge-triggered D flip-flop using NAND gates only. This circuit was simulated on all 4 simulators and the results are given in Table 3.16. Notice that all simulators injected 56 faults (CMOS Version in the case of HITS) and 34-38 classes. When the MOE is evaluated using the coverage given by the simulators, the max MOE falls between 2.3 - 12.8 % as shown in Table 3.16. On the other hand, when the rules are applied and the standard fault coverage is used the MOE is equal to zero as shown in Table 3.17 and Fig. 3.16.

This circuit is a good representative of the rule which unifies the number of classes per simulator. As will be shown later, CADAT gives 2 more classes per primary input (PI) that does not have a

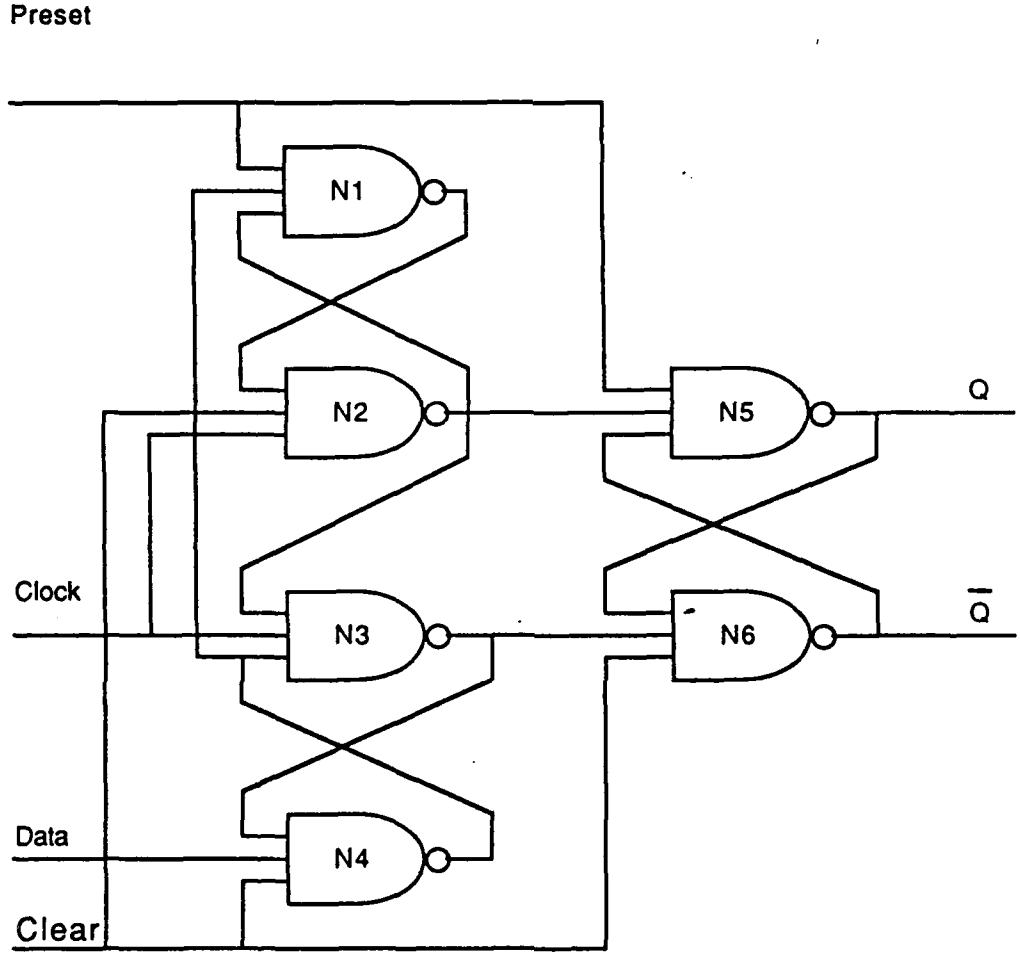



Fig 3.15 Edge-triggered delay flip-flop.

Table 3.16 EDGE-TRIGGERED D-FF

| Step | Number Faults Detected/step | | | | | Number Classes Detected/step | | | | | Cumulative Coverage (%) | | | | | | Cumulative Standard Coverage | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE* % | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE* |
| 1 | 8 | 8 | 6 | 10 | 8 | 5 | 5 | 6 | 7(3)* | 5 | 14.3 | 14.3 | 15.8 | 17.9 | 14.7 | 0.0-3.6 | 14.7 | 14.7 | 14.7 | 14.7 | 14.7 | 0-0 |
| 2** | 36 | 36 | 21 | 35 | 36 | 18 | 19 | 19 | 20(2)* | 18 | 78.6 | 78.6 | 71.1 | 80.4 | 67.6 | 0.0-12.8 | 67.6 | 67.6 | 67.6 | 67.6 | 67.6 | 0-0 |
| 3 | 6 | 6 | 5 | 5 | 6 | 5 | 6 | 5 | 5 | 5 | 89.3 | 89.3 | 84.2 | 89.3 | 82.3 | 0.0-7.0 | 82.3 | 82.3 | 82.3 | 82.3 | 82.3 | 0-0 |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 89.3 | 89.3 | 84.2 | 89.3 | 82.3 | 0.0-7.0 | 82.3 | 82.3 | 82.3 | 82.3 | 82.3 | 0-0 |
| 5 | 1 | 1 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 1 | 91.1 | 91.1 | 89.5 | 92.9 | 85.2 | 0.0-7.7 | 85.3 | 85.3 | 88.2 | 88.2 | 85.2 | 0-3 |
| 6 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 92.9 | 92.9 | 89.5 | 92.9 | 88.2 | 0.0-4.7 | 88.2 | 88.2 | 88.2 | 88.2 | 88.2 | 0-0 |
| 7 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 96.4 | 96.4 | 94.7 | 96.4 | 94.1 | 0.0-2.3 | 94.1 | 94.1 | 94.1 | 94.1 | 94.1 | 0-0 |

| Faults: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | Classes: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Solid Detections: | 54 | 54 | 36 | 54 | 54 | Solid Detections: | 32 | 34 | 34 | 36 | 32 |
| Potential Detections: | 0 | 0 | 0 | 0 | 0 | Potential Detections: | 0 | 0 | 0 | 0 | 0 |
| Undetected: | 2 | 2 | 2 | 2 | 2 | Undetected: | 2 | 2 | 2 | 2 | 2 |
| Total: | 56 | 56 | 38 | 56 | 56 | Total: | 34 | 36 | 36 | 38 | 34 |

** from this point CADAT requires 2 identical vectors per step  * MOE= MARGIN OF ERROR
HILO read twice for each cycle
* Fault classes due to PO fanouts s-a-1 for TTL and s-a-1 & s-a-0 for cmos: To be deleted in computing standard fault coverage.



## Table 3.17 EDGE-TRIGERRED D-FF

| STEPS | MOE BEFORE (%) | MOE AFTER (%) |
|---|---|---|
| 1 | 0.0-3.6 | 0.0-0.0 |
| 2 | 0.0-12.8 | 0.0-0.0 |
| 3 | 0.0-7.0 | 0.0-0.0 |
| 4 | 0.0-7.0 | 0.0-0.0 |
| 5 | 0.0-7.7 | 0.0-3.0 |
| 6 | 0.0-4.7 | 0.0-0.0 |
| 7 | 0.0-2.3 | 0.0-0.0 |

MARGIN OF ERROR BEFORE AND AFTER APPLICATION OF SFC

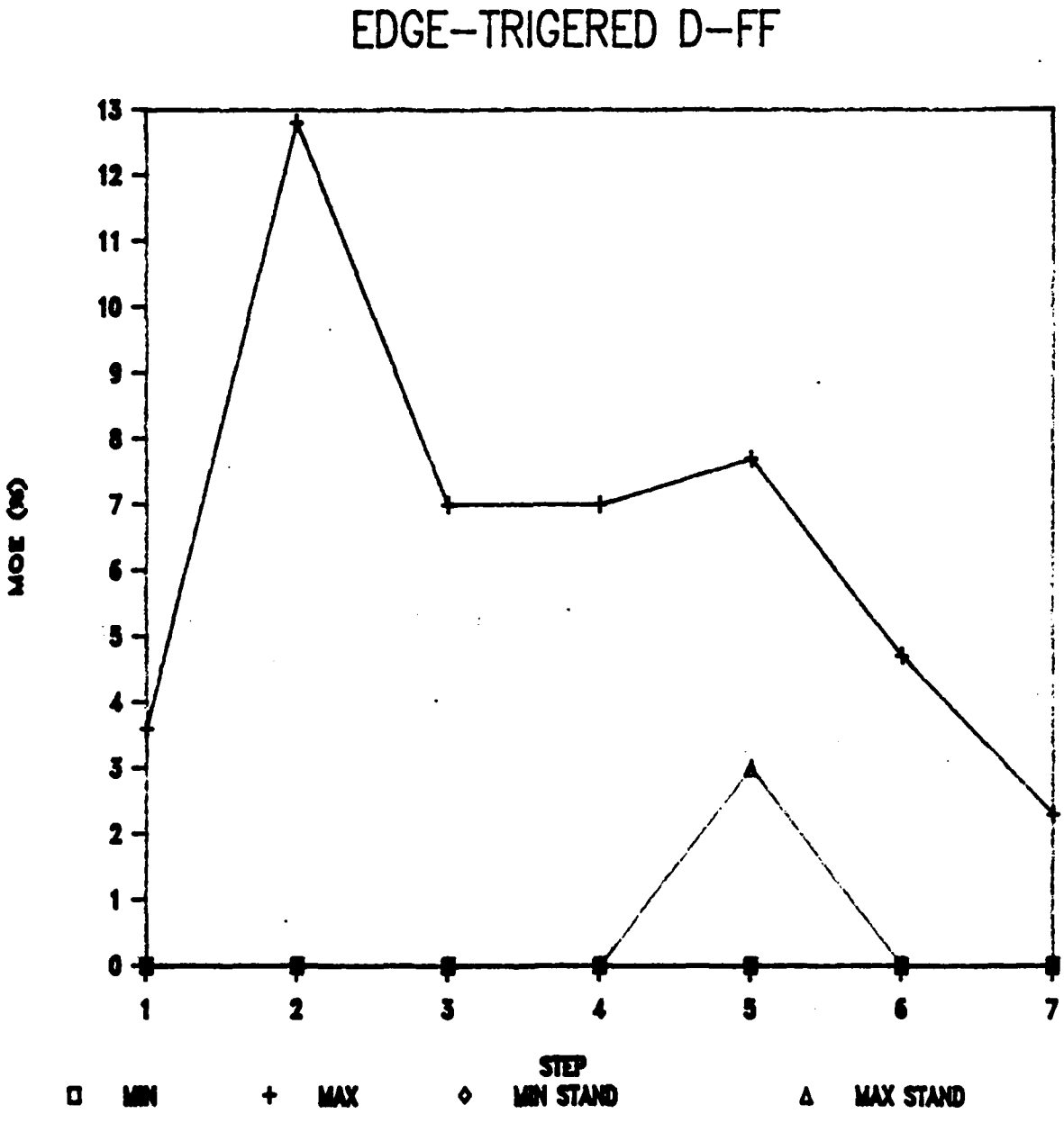

EDGE-TRIGERED D-FF
MOE (SE)
13
12
11
10
9
8
7
6
5
4
3
2
1
0
1
2
3
4
5
6
7
STEP
MIN
MAX
MIN STAND
MAX STAND

Fig. 3.16

fanout, these classes have to be identified and removed from the fault classes list when calculating the standard fault coverage since they collapse to the gate faults. In addition, HITS gives 2 classes per primary output (PO) when a fanout exists at the output. These classes do not exist in the other simulators. Similarly, these classes have to be identified and removed from the fault classes list when calculating the standard fault coverage.

3.3.2.2 TWO FLIP-FLOPS WITH PRESET/CLEAR PLUS AND GATE:

Fig. 3.17 shows this circuit where the PI's are Din, Preset, Clear, and Clock. The MOE before applying the rules is between O.5 - 15% as shown in Tables 3.18 and 3.19. When the fault coverage is evaluated using classes the MOE figure drops by more than half as shown in Table 3.19 and Fig. 3.18. The reason why it does not drop to zero is because of different methods used in fault equivalencing. The following discussion explains it in detail.

As can be seen from Table 3.18, HILO and LASAR have 28 total classes and CADAT has two extra classes due to the PI Din as explained earlier (2.2.2.1). However, HITS has a very interesting feature. Since functionally the output of the flip-flops ($Q_1$ and $Q_2$) will be s–a–o when the CLR line is s-a-o, these faults are members of the same class. While functionally this assumption makes sense, it is not clear why when the PRESET line is s-a-o the faults $Q_1/1$ and $Q_2/1$ do not belong to the same class. Nevertheless, that would make the total classes, in HITS, 26. However, since $Q_2/0$ belongs to the CLR/0 class, the $Q_2$ input to $U_3$ s-a-o will now have a class by itself to make the total number of classes in HITS equal to 27 as given in Table 3.18. This difference, which is true in both calculations, gives a smaller MOE when classes are used in the fault coverage calculation as shown in Table 3.19. It must be noted here that HILO uses buffers for each FF at the PI's and PO in order to inject the faults. Otherwise, the number of faults injected will be much less which again is an optimistic assumption.

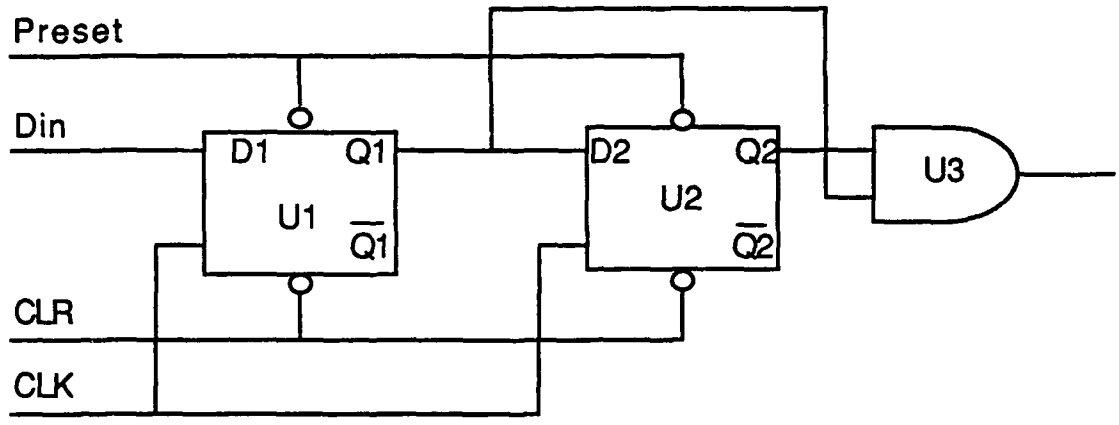



Fig. 3.17 2 FF + AND

TABLE 3.18

2 D-FF's + AND

| | Number Faults Detected/step | | | | | Number Classes Detected/step | | | | | Cumulative Coverage (%) | | | | | | Cumulative Standard Coverage | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Step | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE % | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE % |
| 1 | 8 | 8 | 6 | 9 | 8 | 5 | 5 | 6 | 6 | 5 | 17.9 | 23.5 | 27.3 | 30.0 | 17.9 | 0-12 | 17.9 | 17.9 | 27.7 | 22.2 | 17.9 | 0-4.3 |
| 2 | 2 | 2 | 3 | 3 | 2 | 2 | 2 | 3 | 3 | 2 | 25.0 | 29.4 | 40.9 | 40.0 | 25.0 | 0-15 | 25.0 | 25.0 | 40.9 | 33.3 | 25.0 | 0-8.3 |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 25.0 | 29.4 | 40.9 | 40.0 | 25.0 | 0-15 | 25.0 | 25.0 | 40.9 | 33.3 | 25.0 | 0-8.3 |
| 4 | 8 | 8 | 4 | 6 | 8 | 7 | 7 | 4 | 6 | 7 | 50.0 | 52.9 | 59.1 | 60.0 | 50.0 | 0-10 | 50.0 | 50.0 | 59.0 | 55.6 | 50.0 | 0-5.6 |
| 5 | 12 | 12 | 6 | 9 | 12 | 11 | 12 | 6 | 9 | 11 | 89.3 | 88.2 | 86.4 | 90.0 | 89.3 | .7-1.8 | 89.3 | 89.3 | 86.3 | 88.9 | 89.3 | 0-0.4 |
| 6 | 3 | 3 | 2 | 2 | 3 | 2 | 3 | 2 | 2 | 2 | 96.6 | 97.1 | 95.5 | 96.7 | 96.6 | 0-0.5 | 96.6 | 96.6 | 95.4 | 96.3 | 96.6 | 0-0.3 |

| Faults: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | Classes: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Solid Detections: | 33 | 33 | 21 | 29 | 33 | Solid Detections: | 27 | 29 | 21 | 26 | 27 |
| Potential Detections: | 0 | 0 | 0 | 0 | 0 | Potential Detections: | 0 | 0 | 0 | 0 | 0 |
| Undetectable: | 1 | 1 | 1 | 1 | 1 | Undetectable: | 1 | 1 | 1 | 1 | 1 |
| Undetected: | 0 | 0 | 0 | 0 | 0 | Undetected: | 0 | 0 | 0 | 0 | 0 |
| Total: | 34 | 34 | 22 | 30 | 34* | Total: | 28 | 30 | 22 | 27 | 28* |

* HILO uses buffered D-type flip-flop macros to inject boundary faults



Table 3-19. 2 D-FF's + AND

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.0-12.0 | 0.0-4.3 |
| 2 | 0.0-15.0 | 0.0-8.3 |
| 3 | 0.0-15.0 | 0.0-8.3 |
| 4 | 0.0-10.0 | 0.0-5.6 |
| 5 | 0.7- 1.8 | 0.0-0.4 |
| 6 | 0.0- 0.5 | 0.0-0.3 |

Margin Of Error before and after application of SFC

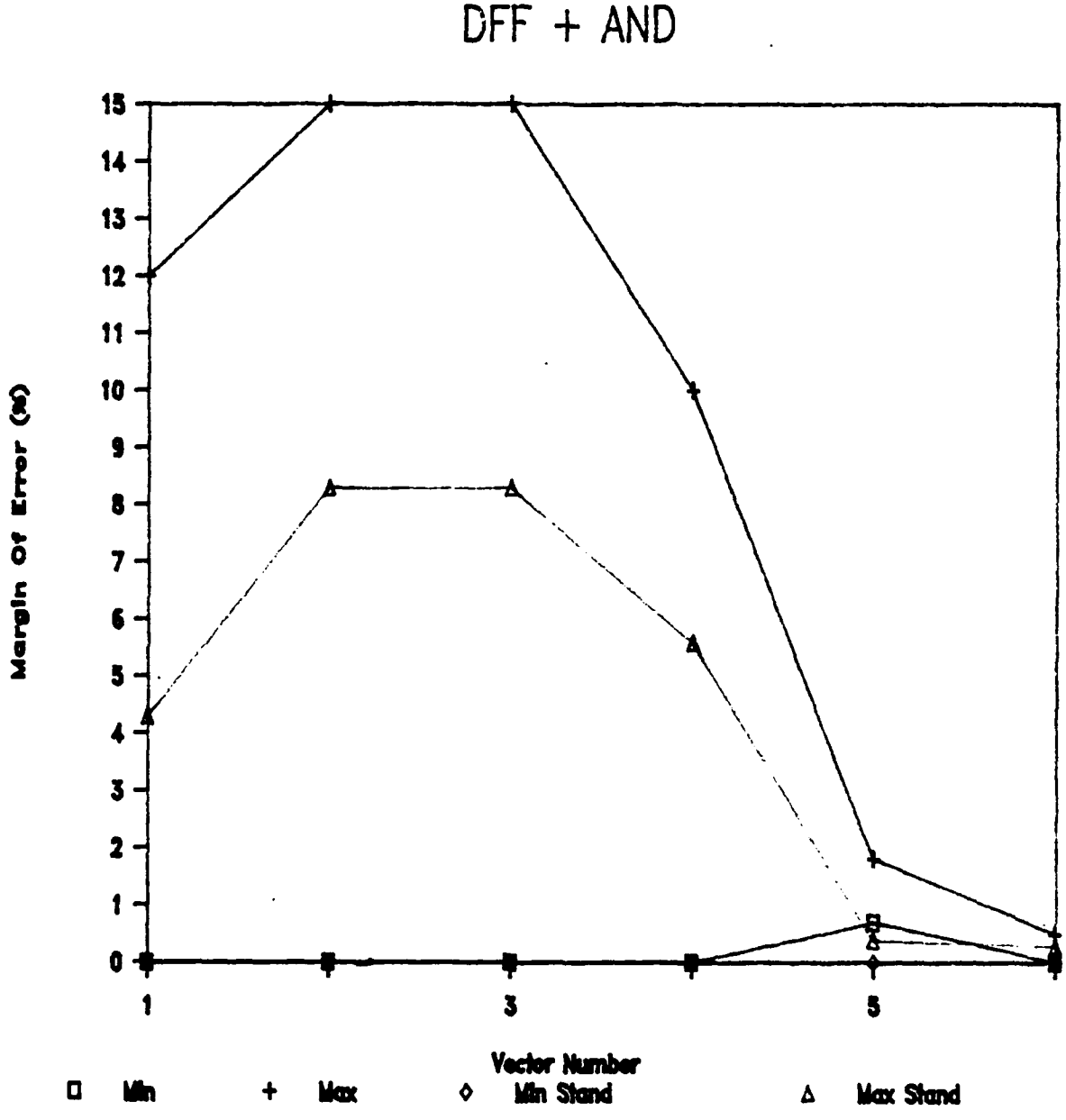

DFF + AND
Margin Of Error (%)
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
1
3
5
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.18

3.3.2.3 FOUR-CASCADED D FLIP-FLOPS:

Fig. 3.19 shows the circuit diagram of 4 cascaded D Flip-Flops with PR and CLR lines. Some observations were encountered with this circuit. First, as in the previous circuit, HILO will not inject faults at each flip-flop line unless a buffer is inserted. When a buffer is inserted at each flip-flop I/0 line, the number of faults injected is consistent with the other simulators and hence the number of classes is 42. LASAR does not have a FF primitive and hence when the FF chip is used the FF internal faults are also injected. CADAT had 2 more classes due to the D PI as mentioned earlier. HITS also uses the functional equivalence of CLR/0 and Qi/0 as in the previous circuit. This accounts for the 39 classes in HITS (CMOS). The test vectors given to each simulator must produce 100% fault coverage. While this was true in CADAT and HITS, as shown in Table 3.20, it was not true in LASAR and HILO. A step by step analysis and trace was followed but no detection was given. The faults which are not detected are Preset and Clear lines s–a–1 in units 2, 3, and 4 (6 faults in HILO undetected, 5 in LASAR since CLR s/1 in unit 2 was detected). It is not understood why these faults are not detected since the test vectors must detect all faults. These test vectors are given in the Appendix. Hence, this error is obviously simulator dependent. Table 3.21 shows the MOE before and after applying the standard fault coverage. Due to the questionable results by HILO and LASAR, no conclusions could be drawn from the results. On the other hand, it may be interesting to note that the minimum difference is smaller after the application of the standard fault coverage as shown in Fig. 3.20. Table 3.22 shows the MOE for CADAT and HITS only and it is clear the standard fault coverage calculation gives a much smaller MOE figure of merit as shown in Fig. 3.21.

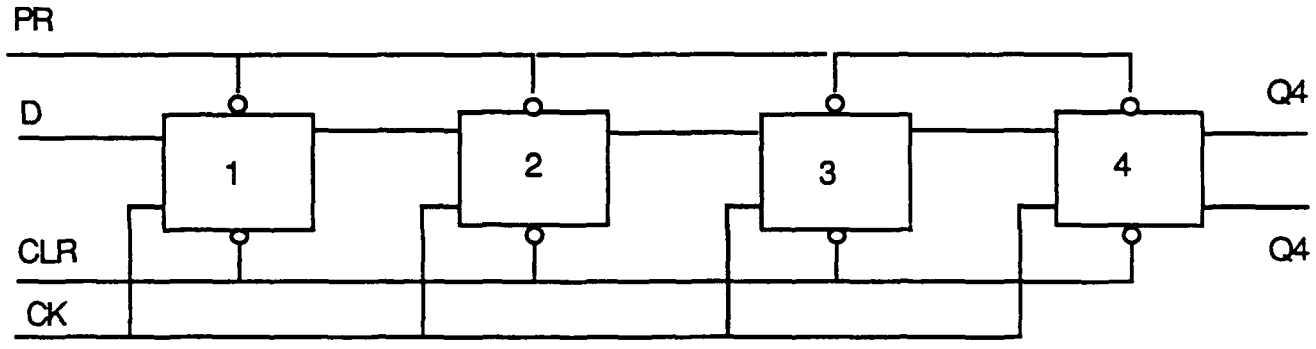



Fig 3.19 Cascaded DFFs

Table 3.20 4 D-FF's CASCADED

| Step | Number Faults Detected/step | | | | | Number Classes Detected/step | | | | | Cumulative Coverage (%) | | | | | | Cumulative Standard Coverage | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE* | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE* |
| 1 | 5 | 4 | 3 | 4 | 2 | 4 | 4 | 3 | 4 | 2 | 8.60 | 8.0 | 10.0 | 9.5 | 4.7 | 0.6- 4.8 | 9.5 | 9.5 | 10.0 | 10.3 | 4.7 | 0.0- 5.6 |
| 2 | 6 | 6 | 5 | 4 | 5 | 5 | 6 | 5 | 6 | 5 | 18.96 | 20.0 | 26.7 | 23.8 | 16.6 | 1.0- 7.2 | 21.4 | 23.8 | 26.6 | 25.6 | 16.6 | 2.4- 9.0 |
| 3 | 4 | 4 | 2 | 3 | 3 | 2 | 3 | 2 | 3 | 2 | 25.80 | 28.0 | 33.3 | 31.0 | 21.4 | 2.2- 9.6 | 26.2 | 31.0 | 33.3 | 33.3 | 21.4 | 1.3-11.9 |
| 4 | 4 | 4 | 2 | 3 | 3 | 2 | 3 | 2 | 3 | 2 | 32.70 | 36.0 | 40.0 | 38.1 | 26.1 | 2.1-12.0 | 31.0 | 38.1 | 40.0 | 41.0 | 26.1 | 1.9-13.9 |
| 5 | 5 | 4 | 2 | 3 | 4 | 3 | 3 | 2 | 3 | 3 | 44.80 | 44.0 | 46.7 | 45.2 | 33.3 | 0.8-11.9 | 38.1 | 45.2 | 46.6 | 48.7 | 33.3 | 1.4-13.3 |
| 6 | 26 | 21 | 10 | 17 | 23 | 19 | 18 | 10 | 14 | 19 | 86.20 | 86.0 | 80.0 | 85.7 | 78.5 | 0.2- 7.7 | 83.3 | 85.7 | 80.0 | 84.6 | 78.5 | 1.5- 7.2 |
| 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 86.20 | 86.0 | 80.0 | 85.7 | 78.5 | 0.2- 7.7 | 83.3 | 85.7 | 80.0 | 84.6 | 78.5 | 1.5- 7.2 |
| 8 | 0 | 2 | 2 | 2 | 1 | 0 | 2 | 2 | 2 | 1 | 86.20 | 90.0 | 86.7 | 90.5 | 80.9 | 0.5- 9.6 | 83.3 | 90.5 | 86.6 | 89.7 | 80.9 | 0.8- 9.6 |
| 9 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 86.20 | 92.0 | 90.0 | 92.9 | 80.9 | 0.9-12.0 | 83.3 | 92.9 | 90.0 | 92.3 | 80.9 | 0.6-10.0 |
| 10 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 86.20 | 94.0 | 93.3 | 95.2 | 80.9 | 0.7-14.3 | 83.3 | 95.2 | 93.3 | 94.9 | 80.9 | 0.3-14.3 |
| 11 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 87.93 | 96.0 | 96.7 | 97.6 | 83.3 | 0.7-14.3 | 85.7 | 97.6 | 96.6 | 97.4 | 83.3 | 0.2-14.3 |
| 12* | 2 | 2 | 1 | 1 | 2 | 1 | 2 | 1 | 1 | 1 | 91.37 | 100. | 100. | 100. | 85.7 | 0.0-14.3 | 88.1 | 100. | 100. | 100. | 85.7 | 0.0-14.3 |

| Faults: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|
| Solid Detections: | 53 | 50 | 30 | 42 | 44 |
| Potential Detections: | 0 | 0 | 0 | 0 | 0 |
| Undetected: | 5 | 0 | 0 | 0 | 6 |
| Total: | 58** | 50 | 30 | 42 | 50*** |

| Classes: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|
| Solid Detections: | 37 | 44 | 30 | 39 | 36 |
| Potential Detections: | 0 | 0 | 0 | 0 | 0 |
| Undetected: | 5 | 0 | 0 | 0 | 6 |
| Total: | 42 | 44 | 30 | 39 | 42* |

* CADAT requires last vector to be repeated.
** LASAR due to addition of buffers in the DFF'S
*** HILO uses 4 buffered D-type flip-flop macros to inject the boundery faults on these macros.

* HILO uses 4 buffered D-type flip-flops macros to inject the boundery faults on these macros
* MOE = Margin Of Error.

Table 3.21 4 DFF'S CASCADED

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.6- 4.8 | 0.0- 5.6 |
| 2 | 1.0- 7.2 | 2.4- 9.0 |
| 3 | 2.2- 9.6 | 1.3-11.9 |
| 4 | 2.1-12.0 | 1.9-13.9 |
| 5 | 0.8-11.9 | 1.4-13.3 |
| 6 | 0.2- 7.7 | 1.5- 7.2 |
| 7 | 0.2- 7.7 | 1.5- 7.5 |
| 8 | 0.5- 9.6 | 0.8- 9.6 |
| 9 | 0.1-12.0 | 0.6-10.0 |
| 10 | 0.7-14.3 | 0.3-14.3 |
| 11 | 0.7-14.3 | 0.2-14.3 |
| 12 | 0.0-14.3 | 0.0-14.3 |

Margin Of Error before and after application of SFC

Table 3.22 4 DFF'S CASCADED
(CADAT and HITS only )

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 1.5 | 0.8 |
| 2 | 3.8 | 1.8 |
| 3 | 3.0 | 2.3 |
| 4 | 2.1 | 1.9 |
| 5 | 1.2 | 3.5 |
| 6 | 0.3 | 1.1 |
| 7 | 0.3 | 1.1 |
| 8 | 0.5 | 0.8 |
| 9 | 0.9 | 0.6 |
| 10 | 1.2 | 0.3 |
| 11 | 1.6 | 0.2 |
| 12 | 0.0 | 0.0 |

Margin Of Error before and after application of SFC

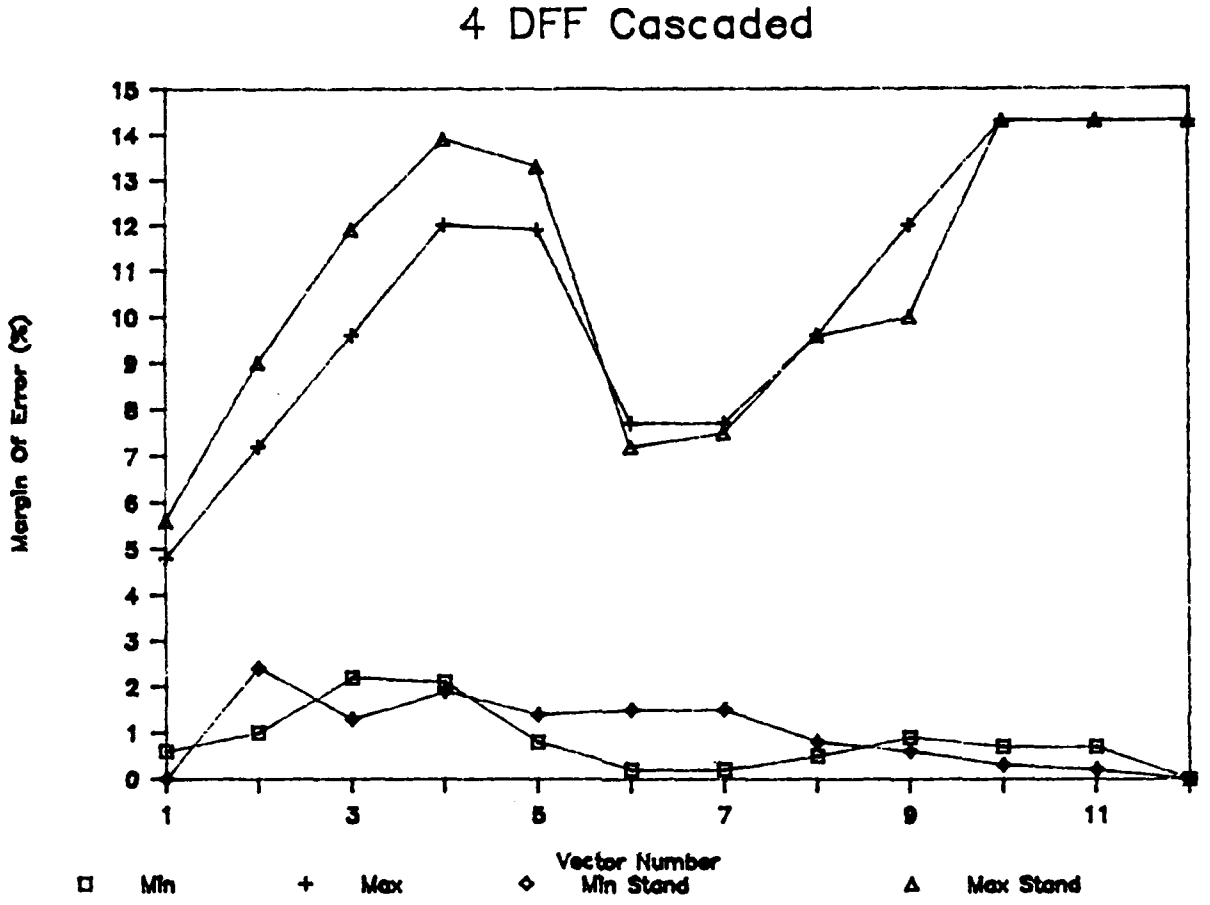

4 DFF Cascaded
Margin Of Error (%)
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
1
3
5
7
9
11
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.20

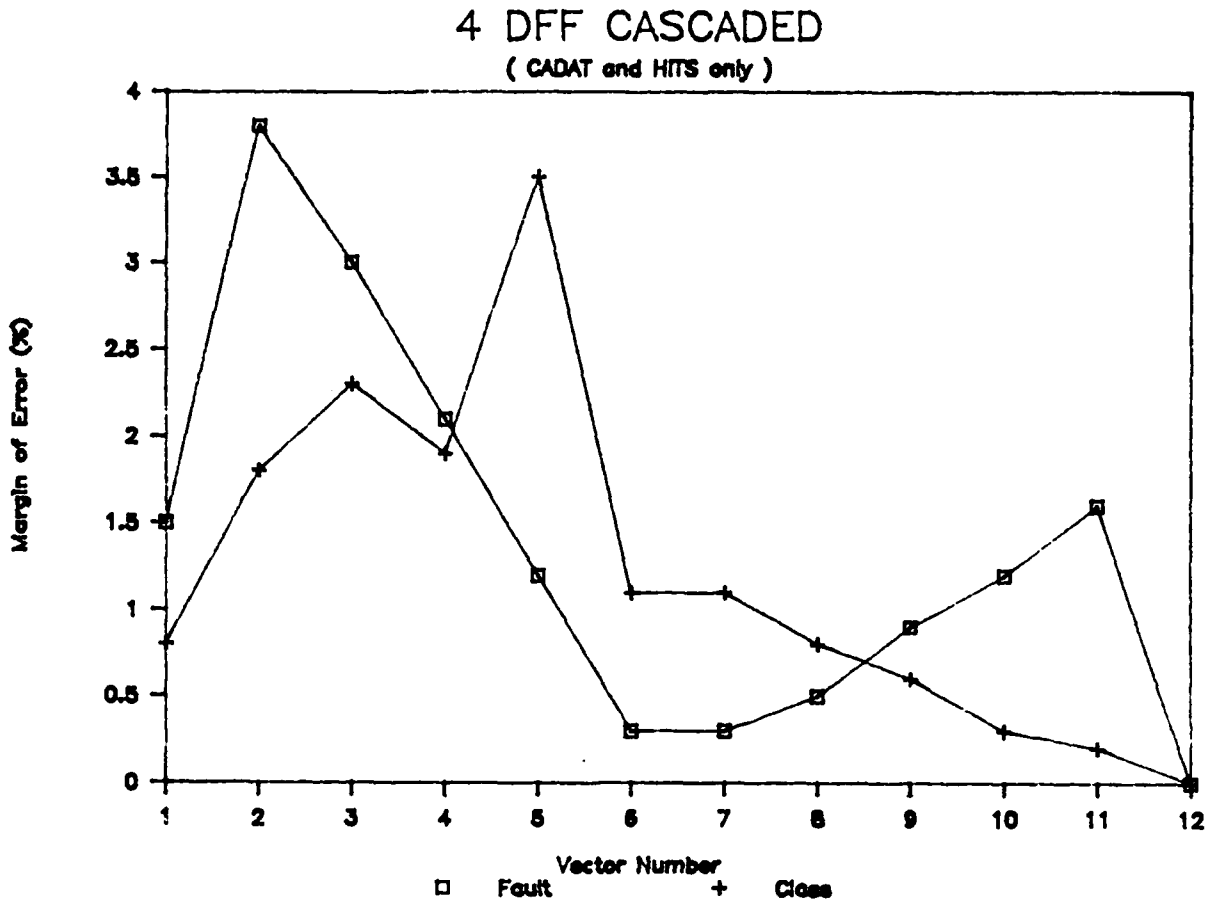

4 DFF CASCADED
( CADAT and HITS only )
Margin of Error (%)
4
3.5
3
2.5
2
1.5
1
0.5
0
1
2
3
4
5
6
7
8
9
10
11
12
Vector Number
Fault
Class

Fig. 3.21

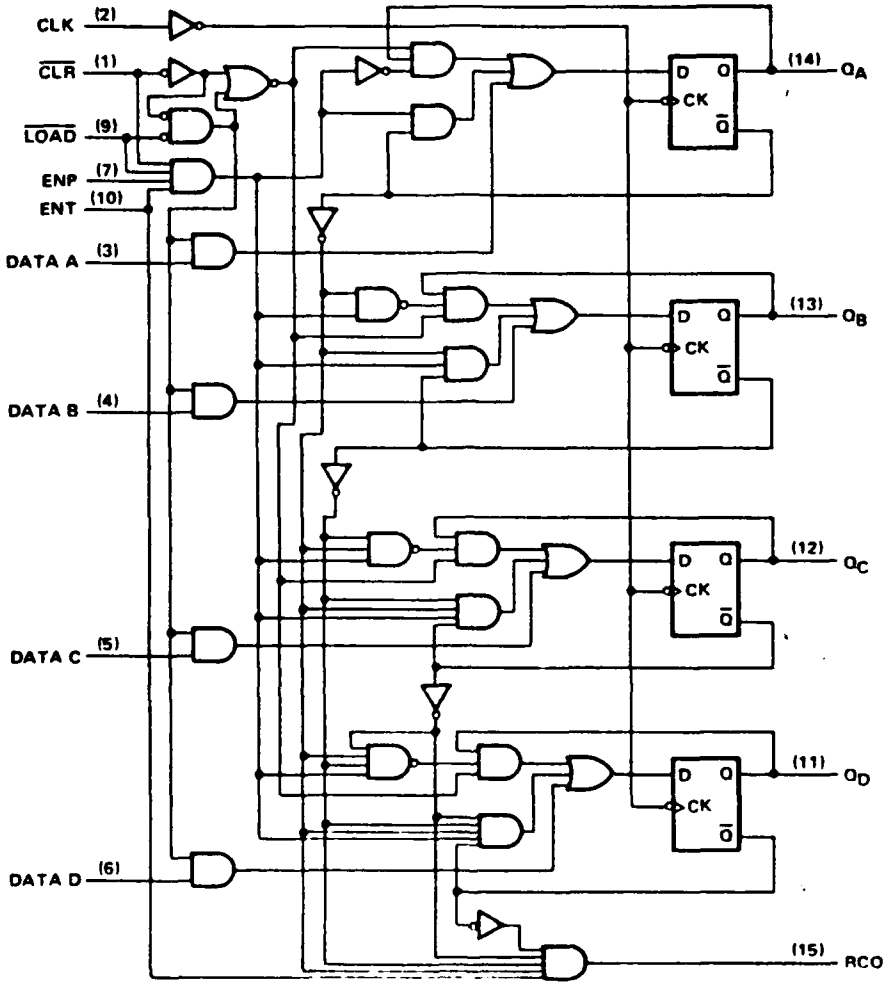



Fig. 3.22 74LS163 Four-Bit Counter

Table 3.23 4-BIT COUNTER 74163

| Step | Number Faults Detected/step LASAR | CADAT | HITS TTL | HITS CMOS | HILO | Number Classes Detected/step LASAR | CADAT | HITS TTL | HITS CMOS | HILO | Cumulative Coverage (%) LASAR | CADAT | HITS TTL | HITS CMOS | HILO | (SOLID ONLY) HOE % |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 70-97 | 38-52 | 21 | 31 | 38-46 | 29-47 | 21-35 | 17 | 22 | 17-25 | 19.8-28.3 | 14.6-20.0 | 13.6 | 14.4 | 13.7-20.2 | 0.2- 6.1 |
| 2 | 120 | 82 | 58 | 77 | 82 | 47 | 33 | 40 | 42 | 32 | 54.1-62.6 | 46.2-51.5 | 51.3 | 50.0 | 39.5-46.0 | 3.8-14.6 |
| 3 | 2 | 2 | 5 | 5 | 2 | 1 | 2 | 3 | 3 | 1 | 54.7-63.3 | 46.9-52.3 | 54.6 | 52.3 | 40.3-46.8 | 2.4-14.4 |
| 4 | 11 | 11 | 11 | 14 | 11 | 10 | 10 | 10 | 12 | 10 | 57.8-66.3 | 51.2-56.5 | 61.7 | 58.8 | 48.4-54.8 | 1.0-10.4 |
| 5 | 8 | 8 | 2 | 2 | 8 | 4 | 6 | 2 | 2 | 4 | 60.1-67.5 | 54.2-59.6 | 63.0 | 59.7 | 51.6-58.1 | 0.4- 8.5 |
| 6 | 20 | 20 | 12 | 16 | 20 | 7 | 7 | 7 | 8 | 7 | 65.7-73.1 | 61.9-67.3 | 70.8 | 67.1 | 57.3-63.7 | 1.4- 9.8 |
| 7 | 11 | 10 | 3 | 8 | 10 | 4 | 4 | 3 | 3 | 4 | 68.8-76.2 | 65.8-71.2 | 72.7 | 70.8 | 60.5-66.9 | 2.0-10.3 |
| 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 68.8-76.2 | 65.8-71.2 | 72.7 | 70.8 | 60.5-66.9 | 2.0-10.3 |
| 9 | 15 | 15 | 7 | 11 | 15 | 5 | 5 | 5 | 5 | 5 | 73.1-80.5 | 71.5-76.9 | 77.3 | 75.9 | 64.5-71.0 | 1.5-11.4 |
| 10 | 2 | 2 | 1 | 2 | 2 | 2 | 2 | 1 | 2 | 2 | 73.7-81.1 | 72.3-77.7 | 77.9 | 76.9 | 66.1-72.6 | 1.4-10.8 |
| 11 | 3 | 3 | 2 | 2 | 3 | 2 | 3 | 2 | 2 | 2 | 74.5-81.9 | 73.5-78.9 | 79.2 | 77.8 | 67.7-74.2 | 1.0-10.1 |
| 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 74.5-81.9 | 73.5-78.9 | 79.2 | 77.8 | 67.7-74.2 | 1.0-10.1 |
| 13 | 10 | 10 | 1 | 1 | 10 | 2 | 3 | 1 | 1 | 2 | 77.3-84.7 | 77.3-82.7 | 79.9 | 78.2 | 69.4-75.8 | 0.0- 8.8 |
| 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 77.3-84.7 | 77.3-82.7 | 79.9 | 78.2 | 69.4-75.8 | 0.0- 8.8 |
| 15 | 11 | 10 | 6 | 9 | 10 | 6 | 6 | 6 | 5 | 6 | 80.5-87.9 | 81.2-86.5 | 83.8 | 82.4 | 74.2-80.6 | 0.7- 8.2 |
| 16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80.7-88.1 | 81.2-86.5 | 83.8 | 82.4 | 74.2-80.6 | 0.7- 8.2 |
| 17 | 1 | 1 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 1 | 80.7-88.1 | 81.5-86.9 | 85.1 | 83.3 | 75.0-81.6 | 0.7- 8.3 |
| 18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 81.3-88.7 | 81.5-86.9 | 85.1 | 83.3 | 75.0-81.6 | 0.2- 8.3 |
| 19 | 2 | 2 | 3 | 4 | 2 | 2 | 2 | 3 | 3 | 2 | 81.3-88.7 | 82.3-87.7 | 87.0 | 85.2 | 76.6-83.1 | 0.2- 8.6 |
| 20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 84.7-92.1 | 82.3-87.7 | 87.0 | 85.2 | 76.6-83.1 | 0.5- 8.6 |
| 21 | 12 | 11 | 3 | 6 | 11 | 6 | 6 | 3 | 3 | 6 | 84.7-92.1 | 86.5-91.9 | 89.0 | 88.0 | 81.5-87.9 | 1.5- 6.5 |
| 22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 85.0-92.4 | 86.9-92.3 | 89.6 | 88.4 | 82.3-88.7 | 1.5- 6.1 |
| 23 | 2 | 2 | 2 | 2 | 2-8 | 2 | 2 | 2 | 2 | 2-4 | 85.6-93.0 | 87.7-93.1 | 90.9 | 89.4 | 83.9-91.9 | 1.7- 5.5 |
| 24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 85.6-93.0 | 87.7-93.1 | 90.9 | 89.4 | 83.9-91.9 | 1.7- 5.5 |
| 25 | 9 | 8 | 1 | 6 | 8 | 2 | 2 | 1 | 1 | 2 | 88.1-95.5 | 90.8-96.2 | 91.6 | 92.1 | 85.5-93.5 | 1.3- 6.6 |
| 26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 88.1-95.5 | 90.8-96.2 | 91.6 | 92.1 | 85.5-93.5 | 1.3- 6.6 |
| 27 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 88.4-95.8 | 91.2-96.5 | 92.2 | 92.6 | 86.3-94.4 | 1.4- 6.3 |
| 28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 88.4-95.8 | 91.2-96.5 | 92.2 | 92.6 | 86.3-94.4 | 1.4- 6.3 |
| 29 | 4 | 4 | 1 | 1 | 4 | 2 | 2 | 1 | 1 | 2 | 89.5-96.9 | 92.7-98.1 | 92.9 | 93.1 | 87.9-96.0 | 0.4- 5.2 |
| 30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 89.5-96.9 | 92.7-98.1 | 92.9 | 93.1 | 87.9-96.0 | 0.4- 5.2 |
| 31 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 89.8-97.2 | 93.1-98.5 | 93.5 | 93.5 | 88.7-96.8 | 0.4- 4.8 |
| 32 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 89.8-97.2 | 93.1-98.5 | 93.5 | 93.5 | 88.7-96.8 | 0.4- 4.8 |
| 33 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 90.1-97.5 | 93.5-98.9 | 94.2 | 94.0 | 89.5-97.6 | 0.5- 4.5 |
| 34 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 90.1-97.5 | 93.5-98.9 | 94.2 | 94.0 | 89.5-97.6 | 0.5- 4.5 |
| 35 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 90.4-97.8 | 93.9-99.2 | 94.2 | 94.0 | 90.3-98.3 | 0.1- 3.7 |
| 36 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 90.4-97.8 | 93.9-99.2 | 94.2 | 94.0 | 90.3-98.3 | 0.1- 3.7 |
| 37 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 90.7-98.1 | 94.2-99.6 | 94.8 | 94.4 | 91.1-99.2 | 0.2- 3.7 |
| 38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 90.7-98.1 | 94.2-99.6 | 94.8 | 94.4 | 91.1-99.2 | 0.2- 3.7 |
| 39 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 90.7-98.1 | 94.6-100. | 94.8 | 94.4 | 91.9-100. | 0.2- 3.9 |

| Faults: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|
| Solid Detections: | 319 | 246 | 146 | 204 | 246 |
| Potential Detections: | 27 | 14 | 0 | 0 | 14* |
| Undetected: | 7 | 0 | 8 | 12 | 0 |
| Total: | 353 | 260 | 154 | 216 | 260** |

* By increasing X detection threshold to 100, HILO reduces the PD from 18 to 14.

** HILO uses buffered DFF macros to inject 16 boundary faults.

| Classes: | LASAR | CADAT | HITS TTL | HITS CMOS | HILO |
|---|---|---|---|---|---|
| Solid Detections: | 140 | 124 | 114 | 124 | 114 |
| Potential Detections: | 18 | 12 | 0 | 0 | 10* |
| Undetected: | 7 | 0 | 6 | 9 | 0 |
| Total: | 165 | 136 | 120 | 133 | 124** |

* By using X detection threshold to 100, HILO reduces the PD classes from 4 to 2.

** HILO uses 4 no-buffered DFF macros and no boundary classes are injected.

Table 3.24 4-BIT COUNTER 74163

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.2- 6.1 | 0.0-3.9 |
| 2 | 3.8-14.6 | 0.0-6.6 |
| 3 | 2.4-14.4 | 0.0-6.9 |
| 4 | 1.0-10.4 | 0.0-8.4 |
| 5 | 0.4- 8.5 | 0.0-6.8 |
| 6 | 1.4- 9.8 | 0.0-7.5 |
| 7 | 2.0-10.3 | 0.0-6.7 |
| 8 | 2.0-10.3 | 0.0-6.7 |
| 9 | 1.6-11.4 | 0.0-6.7 |
| 10 | 1.4-10.8 | 0.0-8.3 |
| 11 | 1.0-10.1 | 0.0-7.1 |
| 12 | 1.0-10.1 | 0.0-7.1 |
| 13 | 0.0- 8.8 | 0.0-6.7 |
| 14 | 0.0- 8.8 | 0.0-6.7 |
| 15 | 0.7- 8.8 | 0.0-7.1 |
| 16 | 0.7- 8.2 | 0.0-7.1 |
| 17 | 0.7- 8.3 | 0.0-8.1 |
| 18 | 0.2- 8.3 | 0.0-8.1 |
| 19 | 0.2- 8.6 | 0.0-9.3 |
| 20 | 0.5- 8.6 | 0.0-9.3 |
| 21 | 1.5- 6.5 | 0.0-8.0 |
| 22 | 1.5- 6.1 | 0.0-8.2 |
| 23 | 1.7- 5.5 | 0.0-8.6 |
| 24 | 1.7- 5.5 | 0.0-8.6 |
| 25 | 1.3- 6.6 | 0.0-8.2 |
| 26 | 1.3- 6.6 | 0.0-8.2 |
| 27 | 1.4- 6.3 | 0.0-8.4 |
| 28 | 1.4- 6.3 | 0.0-8.4 |
| 29 | 0.4- 5.2 | 0.0-8.0 |
| 30 | 0.4- 5.2 | 0.0-8.0 |
| 31 | 0.4- 4.8 | 0.0-8.2 |
| 32 | 0.4- 4.8 | 0.0-8.2 |
| 33 | 0.5- 4.5 | 0.0-7.6 |
| 34 | 0.5- 4.5 | 0.0-7.6 |
| 35 | 0.1- 3.7 | 0.0-7.8 |
| 36 | 0.1- 3.7 | 0.0-7.8 |
| 37 | 0.2- 3.7 | 0.0-7.1 |
| 38 | 0.2- 3.7 | 0.0-7.1 |
| 39 | 0.2- 3.9 | 0.0-7.1 |

Margin Of Error before and after application of SFC

Table 3.25 4-BIT COUNTER 74163

(MOE CALC WITHOUT LASAR)

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 0.2-0.9 | 0-0.7 |
| 2 | 3.8-10.5 | 0-5.3 |
| 3 | 5.4-12.0 | 0-6.9 |
| 4 | 2.8-10.4 | 0-8.4 |
| 5 | 2.6-8.1 | 0-6.8 |
| 6 | 4.6-9.8 | 0-7.5 |
| 7 | 5.0-10.3 | 0-6.7 |
| 8 | 5.0-10.3 | 0-6.7 |
| 9 | 4.4-11.4 | 0-6.7 |
| 10 | 4.6-10.8 | 1.6-8.3 |
| 11 | 4.3-10.1 | 0-6.7 |
| 12 | 4.3-10.1 | 0-6.7 |
| 13 | 0.9-8.8 | 0-5.8 |
| 14 | 0.9-8.8 | 0-5.8 |
| 15 | 1.2-8.2 | 0-5.0 |
| 16 | 1.2-8.2 | 0-5.0 |
| 17 | 1.8-8.3 | 0-5.8 |
| 18 | 1.8-8.3 | 0-5.8 |
| 19 | 2.9-8.6 | 0-6.6 |
| 20 | 2.9-8.6 | 0-6.6 |
| 21 | 1.5-6.5 | 0-4.1 |
| 22 | 1.5-6.5 | 0-4.1 |
| 23 | 1.7-5.5 | 0-4.1 |
| 24 | 1.7-5.5 | 0-4.1 |
| 25 | 1.3-6.6 | 0-3.3 |
| 26 | 1.3-6.6 | 0-3.3 |
| 27 | 1.4-6.3 | 0-3.3 |
| 28 | 1.4-6.3 | 0-3.3 |
| 29 | 0.4-5.2 | 0-2.5 |
| 30 | 0.4-5.2 | 0-2.5 |
| 31 | 0.4-4.8 | 0-2.5 |
| 32 | 0.4-4.8 | 0-2.5 |
| 33 | 0.5-4.5 | 0-1.7 |
| 34 | 0.5-4.5 | 0-1.7 |
| 35 | 0.1-3.7 | 0-1.7 |
| 36 | 0.1-3.7 | 0-1.7 |
| 37 | 0.2-3.3 | 0-0.9 |
| 38 | 0.2-3.3 | 0-0.9 |
| 39 | 0.2-2.7 | 0-0.1 |

Margin of Error before and after application of SFC

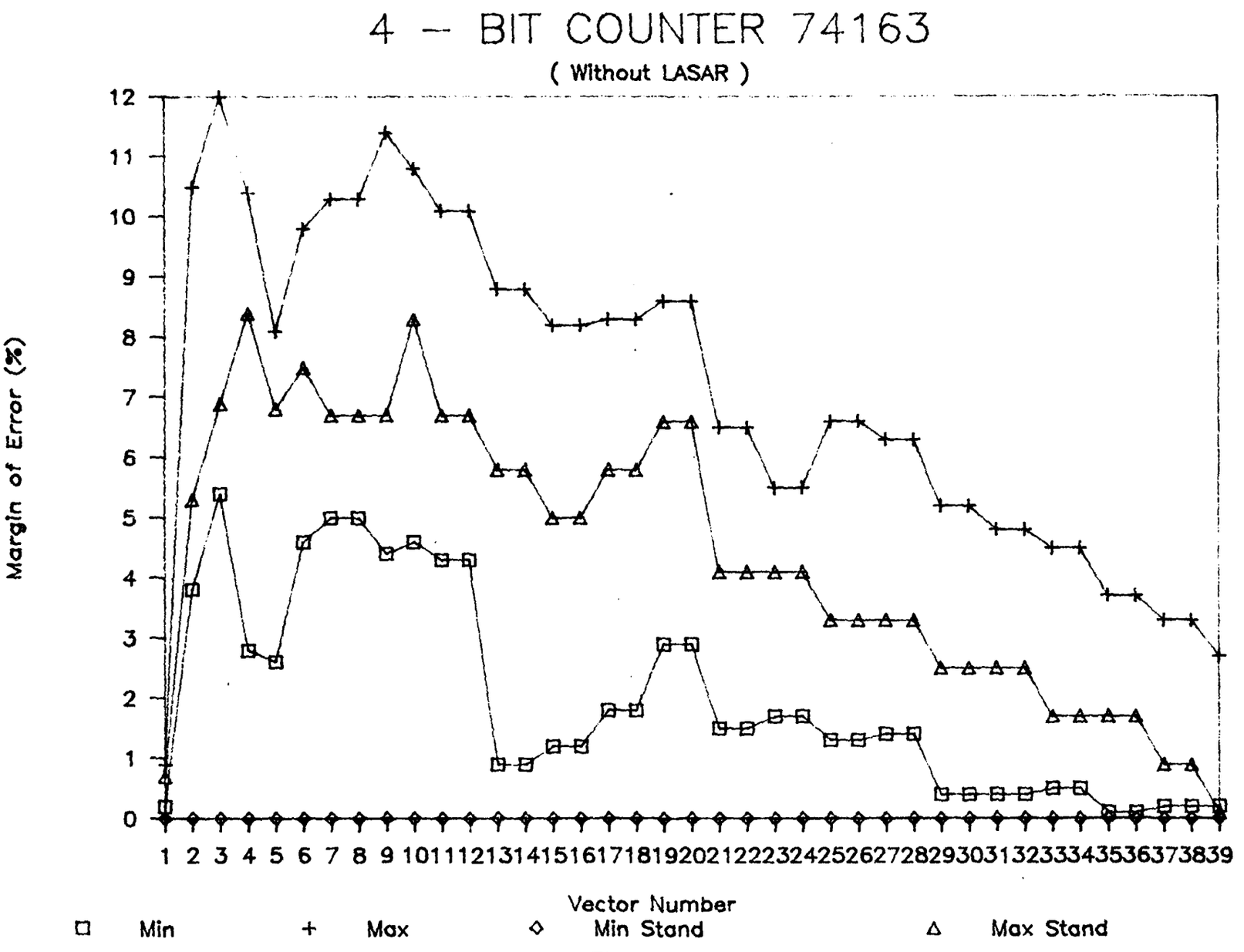

4 – BIT COUNTER 74163
( Without LASAR )
Margin of Error (%)
0
1
2
3
4
5
6
7
8
9
10
11
12
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
Vector Number
Min
Max
Min Stand
Max Stand

Fig. 3.23

3.3.2.4 FOUR-BIT BINARY COUNTER (74LS163):

Fig. 3.22 shows the synchronous four-bit binary counter with 9 PI's and 5 PO's (4 bits and carry out). Thirty nine vectors were used in this circuit where some of the vectors were used for initialization as shown in Table 3.23. HILO uses 4 D FFs with no buffers since we are only interested in injecting faults at the input D and clock lines. It is assumed that there are no Clear or Preset lines available. Because the FFs cannot be initialized, all CLOCK line faults are potentially detected as Table 3.23 shows in the case of LASAR, CADAT, and HILO. LASAR, as mentioned earlier, does not have a D FF primitive, therefore, when a chip is used for the D FF, all internal faults are included. That accounts for having more faults injected in the circuit. However, the number of additional classes will be much less since many of these faults are equivalent. HITS will not consider potential faults for clock lines and will report them as undetected. Because of these added faults in LASAR the MOE does not decrease as shown in Table 3.24 although the minimum is always zero. However, if LASAR's results are removed, the MOE drops dramatically as shown in Table 3.25 and Fig. 3.23.

3.3.2.5. FOUR-BIT SHIFT REGISTER (74LS195):

Fig. 3.24 shows the circuit diagram for the 4-bit shift register with 9 PI's and 5 PO's. There are nine PI's with no fan-out in the diagram. Hence, the number of unique classes are 87 (In CADAT: 105-9x2=87). However, in the case of HITS, several faults (and hence classes) are functionally equivalent when the CLR line is s/0 and therefore, the number of classes are less. In LASAR no faults at the FF level were used so that one could study the other extreme (the first extreme being all flip-flop internal faults included). While CADAT gave 100% coverage, HITS missed one fault which is $Q_A$ s/1. After careful analysis, it seems that the simulator has an error since there is no reason not to detect this fault. This analysis is shown in Fig. 3.26 for both the faulty and fault-free behavior using

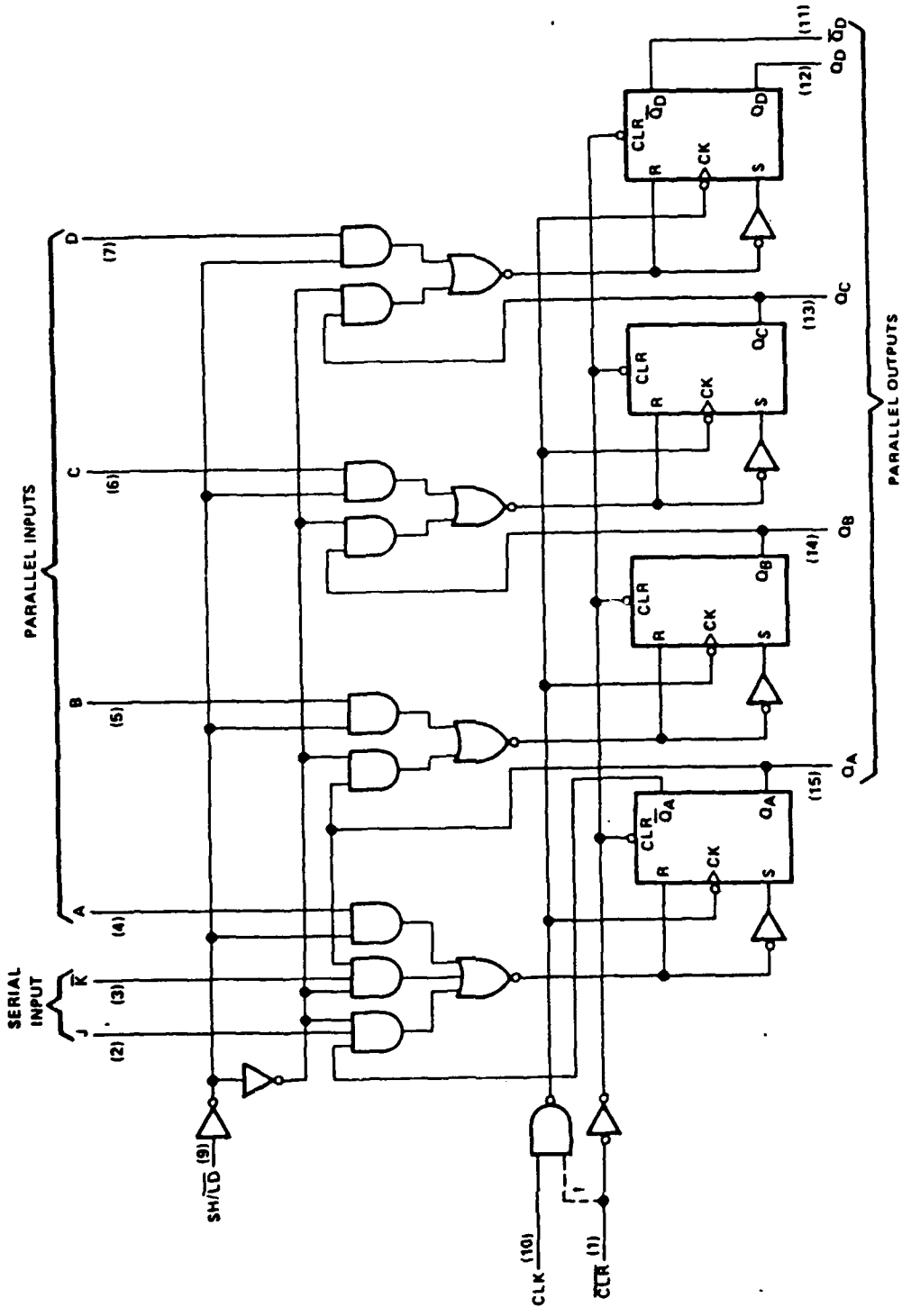



Fig. 3.24 Four Bit Shift Register
(74ls195)

Table 3.26 4-BIT SHIFTER 74195

| Step | Number Faults Detected/step LASAR | CADAT | HITS | HILO | Number Classes Detected/step LASAR | CADAT | HITS | HILO | Cumulative Coverage (%) LASAR | CADAT | HITS TTL | HITS CMOS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 9-12 | 12 | 14 | 5 | 9-10 | 11 | 13 | 5 | 6.2- 8.3 | 6.7 | 13.3 | 13.3 |
| 2 | 29 | 42 | 21 | 42-45 | 10 | 16 | 12 | 12-13 | 26.2-28.3 | 30.3 | 33.3 | 30.8 |
| 3 | 0 | 0 | 0* | 0-1 | 0 | 0 | 0 | 0-1 | 26.2-28.3 | 30.3 | 33.3 | 30.8 |
| 4 | 33 | 35 | 24 | 35-36 | 15 | 23 | 16 | 18-19 | 46.2-48.2 | 50.0 | 56.2 | 50.4 |
| 5 | 3 | 49 | 27 | 49-51 | 14 | 30 | 19 | 25-27 | 68.9-71.0 | 77.5 | 81.9 | 77.6 |
| 6 | 4 | 7 | 4 | 7 | 2 | 6 | 4 | 6 | 71.0-73.1 | 81.5 | 85.7 | 82.5 |
| 7 | 7 | 9 | 2 | 9 | 2 | 3 | 2 | 3 | 73.8-75.9 | 86.5 | 87.6 | 87.4 |
| 8 | 4 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 78.6-80.7 | 86.5 | 87.6 | 87.4 |
| 9 | 0 | 4 | 3 | 4 | 3 | 4 | 3 | 3 | 81.4-83.5 | 88.8 | 90.5 | 89.5 |
| 10 | 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 81.4-83.5 | 88.8 | 90.5 | 89.5 |
| 11 | 2 | 9 | 3 | 9 | 5 | 5 | 3 | 4 | 89.7-91.8 | 93.8 | 93.3 | 93.0 |
| 12 | 0 | 3 | 2 | 3 | 2 | 3 | 2 | 3 | 91.0-93.1 | 95.5 | 95.2 | 95.1 |
| 13 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 91.0-93.1 | 95.5 | 95.2 | 95.1 |
| 14 | 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 92.4-94.5 | 96.6 | 97.1 | 96:5 |
| 15 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 92.4-94.5 | 96.6 | 97.1 | 96.5 |
| 16* | 6 | 6 | 2 | 6 | 1 | 2 | 2 | 1 | 93.1-95.2 | 100.0 | 99.1 | 99.3 |

| Faults: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 140 | 178 | 104 | 171 |
| Potential Detections: | 3 | 0 | 0 | 7 |
| Undetected: | 2 | 0 | 1** | 0 |
| Total: | 145 | 178 | 105 | 178*** |

* CADAT requires last vector to be repeated.
** This fault #1-7 should be detected at step#11
*** HILO uses 4 buffered J-K flip-flop macros to inject the boundary faults on these macros.

| Cumulative Standard Coverage HILO | MOE* | LASAR | CADAT | HITS TTL | HITS CMOS | HILO | MOE* |
|---|---|---|---|---|---|---|---|
| 5.7 | 1.0- 7.6 | 13.0-14.5 | 11.5 | 16.6 | 17.0 | 5.7 | 2.5-11.3 |
| 19.5-20.6 | 0.5-10.2 | 27.5-28.5 | 25.3 | 32.0 | 30.7 | 19.5-20.6 | 3.2-10.1 |
| 19.5-21.7 | 0.5-11.6 | 27.5-28.5 | 25.3 | 32.0 | 30.7 | 19.5-21.6 | 3.2- 9.1 |
| 40.2-43.6 | 0.4- 6.8 | 49.3-50.8 | 46.0 | 52.5 | 50.0 | 40.2-43.6 | 0.8- 7.2 |
| 68.9-74.6 | 0.1- 6.6 | 69.6-71.1 | 74.7 | 76.9 | 75.0 | 68.9-74.6 | 0.1- 3.9 |
| 75.8-81.5 | 0- 9.4 | 72.5-74.0 | 81.6 | 82.0 | 81.8 | 75.8-81.5 | 0.1- 7.8 |
| 79.3-85.0 | 0.9-11.5 | 75.3-76.8 | 85.1 | 84.6 | 85.2 | 79.3-85.0 | 0.1- 8.4 |
| 79.3-85.0 | 0.9- 6.7 | 76.8-78.3 | 85.1 | 84.6 | 85.2 | 79.3-85.0 | 0.1- 6.9 |
| 82.7-88.4 | 0.4- 6.6 | 81.2-82.6 | 88.5 | 88.4 | 88.6 | 82.7-88.4 | 0.1- 6.0 |
| 82.7-88.4 | 0.4- 6.0 | 81.2-82.6 | 88.5 | 88.4 | 88.6 | 82.7-88.4 | 0.1- 6.0 |
| 87.3-93.0 | 0- 2.0 | 88.4-89.9 | 93.1 | 91.0 | 92.0 | 87.3-93.0 | 0.1- 3.2 |
| 90.8-96.5 | 0.4- 3.4 | 91.3-92.8 | 96.6 | 93.5 | 95.5 | 90.8-96.5 | 0.1- 3.8 |
| 90.8-96.5 | 0.4- 3.4 | 91.3-92.8 | 96.6 | 93.5 | 95.5 | 90.8-96.5 | 0.1- 3.8 |
| 93.1-98.8 | 0.1- 4.3 | 94.3-95.8 | 98.9 | 96.1 | 97.7 | 93.1-98.8 | 0.1- 3.1 |
| 93.1-98.8 | 0.1- 4.3 | 94.3-95.8 | 98.9 | 96.1 | 97.7 | 93.1-98.8 | 0.1- 3.1 |
| 94.2-100. | 0- 4.8 | 95.8-97.3 | 100.0 | 98.7 | 98.9 | 94.2-100. | 0- 2.7 |

| Classes: | LASAR | CADAT | HITS | HILO |
|---|---|---|---|---|
| Solid Detections: | 66 | 105 | 77 | 82 |
| Potential Detections: | 1 | 0 | 0 | 5 |
| Undetected: | 2 | 0 | 1** | 0 |
| Total: | 69 | 105 | 78 | 87*** |

* Higher coverage due to clock application & PO #5 which is combinational
** This calss should be detected at step #11
*** HILO uses 4 buffered J-K flip-flop macros to inject the boundary faults.
* MOE = Margin Of Error

Table 3.27 SHIFTER 74195

| Step | MOE Before (%) | MOE After (%) |
|---|---|---|
| 1 | 1.0- 7.6 | 2.5-11.3 |
| 2 | 0.5-10.2 | 3.2-10.1 |
| 3 | 0.5-11.6 | 3.2- 9.1 |
| 4 | 0.4- 6.8 | 0.8. 7.2 |
| 5 | 0.1- 6.6 | 0.1- 3.9 |
| 6 | 0- 9.4 | 0.1- 7.8 |
| 7 | 0.9-11.5 | 0.1- 8.4 |
| 8 | 0.9- 6.7 | 0.1- 6.9 |
| 9 | 0.4- 6.0 | 0.1- 6.0 |
| 10 | 0.4- 6.0 | 0.1- 6.0 |
| 11 | 0- 2.0 | 0.1- 3.2 |
| 12 | 0.4- 3.4 | 0.1- 3.8 |
| 13 | 0.4- 3.4 | 0.1- 3.8 |
| 14 | 0.1- 4.3 | 0.1- 3.1 |
| 15 | 0.1- 4.3 | 0.1- 3.1 |
| 16 | 0- 4.8 | 0- 2.7 |

Margin Of Error before and after application of SFC

Fig. 3.25 Shifter 74195

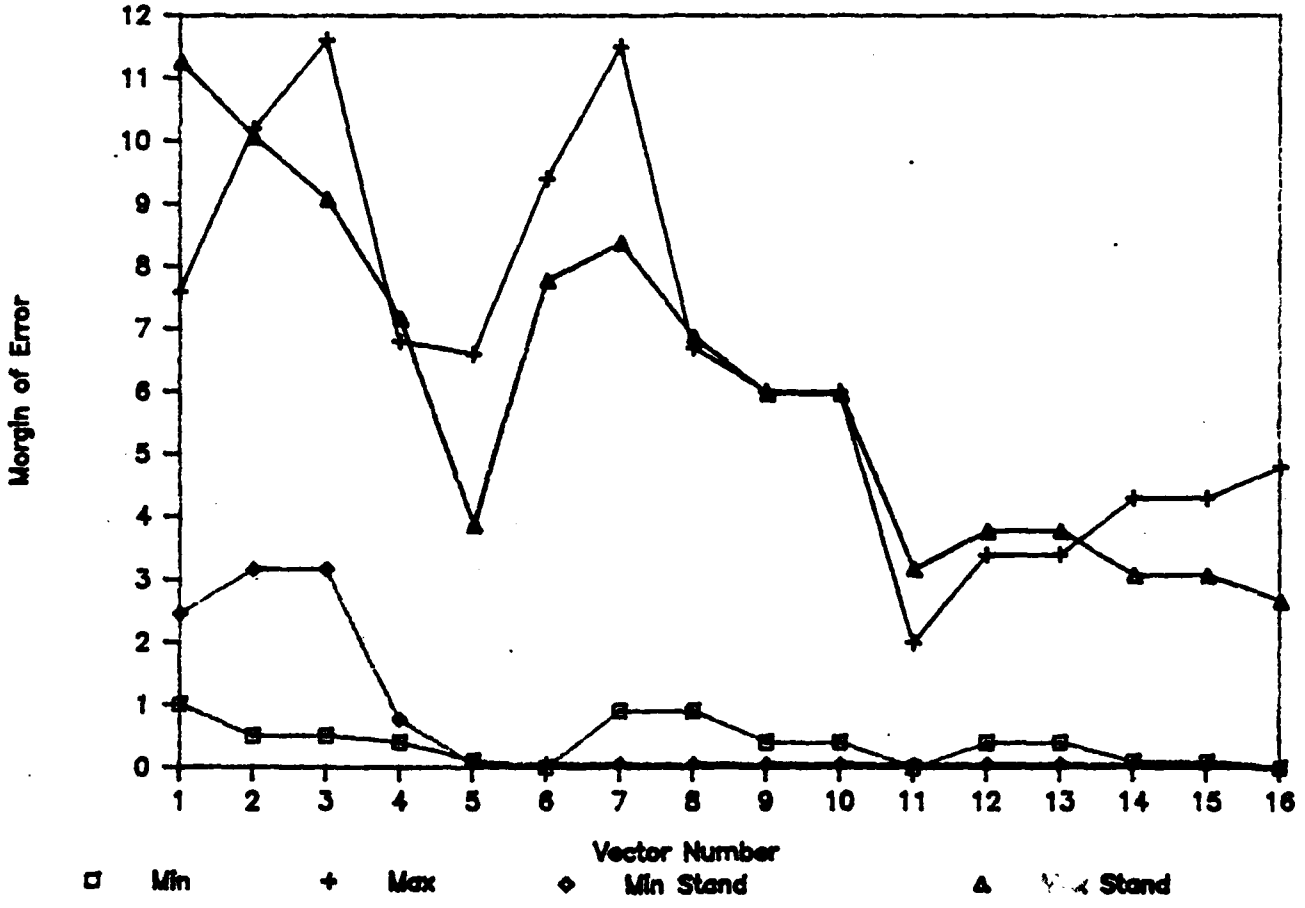
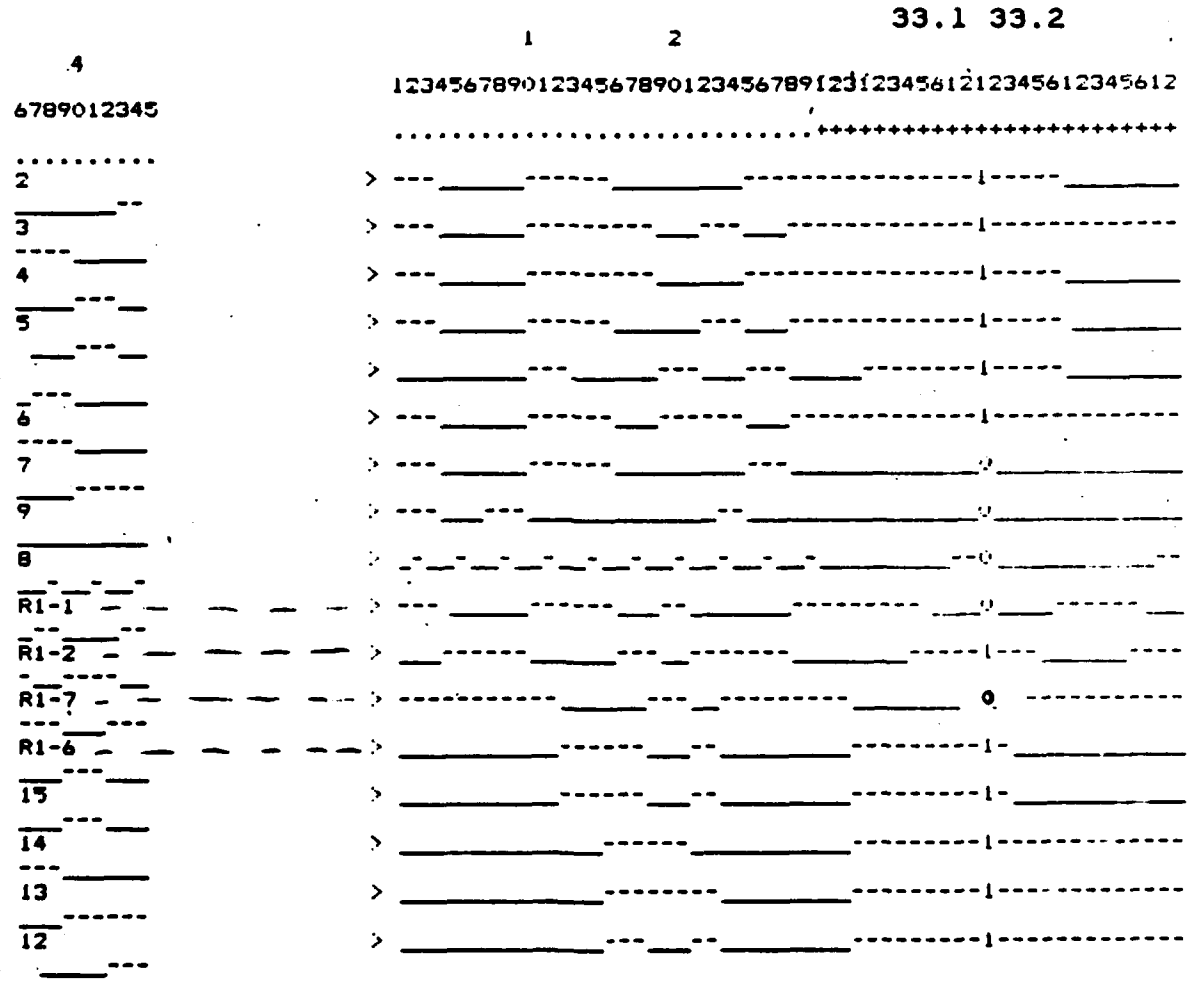


Fig. 3.26 4-bit shift analysis in HITS (step by step detection)

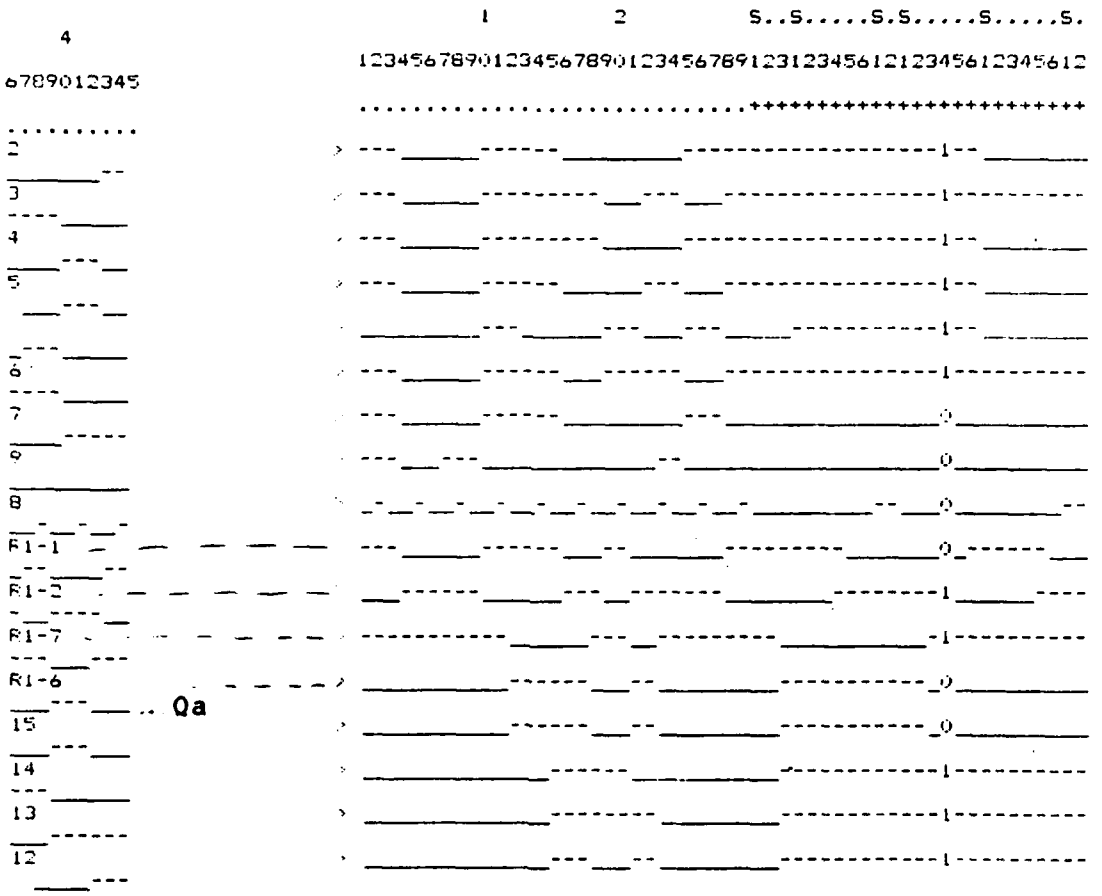
(a) Faulty Behavior




For faulty behavior Qa (R1-6) =1 when it is s@1.

[ In the fault report this fault is declared undetected, although the response of the fault-free and the faulty circuit is clearly opposite as shown in fig.3.26(a) &(b).]

(b) Fault-Free Behavior




Fault-Free behavior Qa =0 as shown

For faulty behavior Qa =1 when Not Q of unit 1 is stuck at 1

the single step feature of HITS. The unit in question is R1-6 which is QA in Fig. 3.26 (i.e. the undetected node).

HILO uses 4 buffered flip-flops to inject boundary faults to the FFs. Once again 5 faults were not detected solidly but rather declared potentially detected. After careful analysis, no determination was made on why HILO did not detect them solidly. One reason perhaps is because they are declared potentially detected early and hence they are removed from the fault list even though they may be solidly detected later on. LASAR uses flip-flops with no faults injected internally, and still it is not clear why 2 classes were not detected. One of the features of LASAR is that it has 2 options. Each option has its advantages but both cannot be called simultaneously, and hence, the ability to take advantage of both is limited. These options are Efaults and Faultput. While one injects all faults in the circuit, it does not provide any information concerning the classes while the other one does but excludes some faults. Table 3.27 and Fig. 3.25 give the MOE before and after the application of the standard fault coverage. The results here may be inconclusive due to the fact that several faults were supposed to be detected in HILO and other classes in LASAR were not included as stated above. Even then, the results of the MOE is smaller.

## 3.4 CONCLUSION

This chapter presented simulated results for the four simulators on 10 different circuits. Although, it was clear that each simulator has its own features, strengths and weaknesses, our task was to evaluate these simulators, observe their behavior and recommend some rules or procedure that would allow for a better correlation. These rules or guidelines will be discussed in detail in the next chapter. However, it was shown from the results presented in this chapter that our figure of merit (Margin Of Error) decreases if the fault classes are used in evaluating the fault coverage instead of total injected faults. Tables 3.28 and 3.29 show the MOE results for the combinational and sequential test circuits, respectively.

Combinational Test Circuits

TABLE 3.28

| Steps | XNOR MOE Before* | XNOR MOE After* | Gray Code Converter MOE Before* | Gray Code Converter MOE After* | 2-Bit Adder MOE Before* | 2-Bit Adder MOE After* | 4-Bit Computer (7485) MOE Before* | 4-Bit Computer (7485) MOE After* | ALU (74181) MOE Before* | ALU (74181) MOE After* |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0-7.7 | 0-0 | 0-1.0 | 0-0.3 | 0-6.0 | 0-6.3 | 0-6.3 | 0-0 | 0.2-5.6 | 0.3-8.7 |
| 2 | 0-6.0 | 0-0 | 0-3.2 | 0-0.6 | 1-1.0 | 0-2.6 | 0-7.5 | 0-0 | 0.0-10.2 | 0.5-9.3 |
| 3 | 0-2.1 | 0-0 | 0-1.9 | 0-0.7 | 0-1.7 | 0-2.2 | 0-6.1 | 0-0 | 0.1-10.6 | 0.3-8.5 |
| 4 | 0-0 | 0-0 | 0-3.3 | 0-0.9 | 0-9.0 | 0-2.3 | 0-6.8 | 0-0 | 0.3-7.1 | 0.2-6.0 |
| 5 | | | | | 0-3.7 | 0-.8 | 0-6.4 | 0-0 | 0.1-6.6 | 0.0-4.6 |
| 6 | | | | | 0-0 | 0-0 | 0-6.4 | 0-0 | 1.1-7.5 | 0.2-3.5 |
| 7 | | | | | | | 0-5.1 | 0-0 | 0.3-5.4 | 0.2-3.3 |
| 8 | | | | | | | 0-3.5 | 0-0 | 1.5-6.8 | 0.3-2.8 |
| 9 | | | | | | | 0-2.3 | 0-0 | 0.4-6.4 | 1.0-2.4 |
| 10 | | | | | | | 0-1.8 | 0-0 | 1.1-5.2 | 0.9-2.6 |
| 11 | | | | | | | 0-4.8 | 0-0 | 0.7-5.4 | 0.2-2.5 |
| 12 | | | | | | | 0-4.5 | 0-0 | 1.5-4.0 | 0.2-1.9 |
| 13 | | | | | | | 0-4.1 | 0-0 | 0.3-3.4 | 0.2-2.2 |
| 14 | | | | | | | 0-3.7 | 0-0 | 0.2-2.7 | 0.1-1.8 |
| 15 | | | | | | | 0-3.4 | 0-0 | 0.0-2.5 | 0.0-1.8 |
| 16 | | | | | | | 0-3.0 | 0-0 | | |
| 17 | | | | | | | 0-2.7 | 0-0 | | |
| 18 | | | | | | | 0-2.2 | 0-0 | | |
| 19 | | | | | | | 0-1.9 | 0-0 | | |
| 20 | | | | | | | 0-1.6 | 0-0 | | |
| 21 | | | | | | | 0-1.1 | 0-0 | | |
| 22 | | | | | | | 0-0.8 | 0-0 | | |
| 23 | | | | | | | 0-0.2 | 0-0 | | |
| 24 | | | | | | | 0-0 | 0-0 | | |

* Before and After Application of Standard Fault Coverage

## Sequential Test Circuits

TABLE 3.29

| | E-T DFF | | 2 DFF + AND | | 4 DFF Cascaded** | | 4-Bit Counter (74163) | | 4-Bit Shifter (74195) | |
|---|---|---|---|---|---|---|---|---|---|---|
| Steps | MOE Before* | MOE After* | MOE Before* | MOE After* | MOE Before* | MOE After* | MOE Before* | MOE After* | MOE Before* | MOE After* |
| 1 | 0-3.6 | 0-0 | 0-12.0 | 0-4.3 | 1.5 | 0.8 | 0.2-0.9 | 0-0.7 | 1.0-7.6 | 2.5-11.3 |
| 2 | 0-12.8 | 0-0 | 0-15.0 | 0-8.3 | 3.8 | 1.8 | 3.8-10.5 | 0-5.3 | 0.5-10.2 | 3.2-10.1 |
| 3 | 0-7.0 | 0-0 | 0-15.0 | 0-8.3 | 3.0 | 2.3 | 5.4-12.0 | 0-6.9 | 0.5-11.6 | 3.2-9.1 |
| 4 | 0-7.0 | 0-0 | 0-10.0 | 0-5.6 | 2.1 | 1.9 | 2.8-10.4 | 0-8.4 | 0.4-6.8 | 0.8-7.2 |
| 5 | 0-7.7 | 0-3.0 | 0.7-1.8 | 0-0.4 | 1.2 | 3.5 | 2.6-8.1 | 0-6.8 | 0.1-6.6 | 0.1-3.9 |
| 6 | 0-4.7 | 0-0 | 0-0.5 | 0-0.3 | 0.3 | 1.1 | 4.6-9.8 | 0-7.5 | 0.0-9.4 | 0.1-7.8 |
| 7 | 0-2.3 | 0-0 | | | 0.3 | 1.1 | 5.0-10.3 | 0-6.7 | 0.9-11.5 | 0.1-8.4 |
| 8 | | | | | 0.5 | 0.8 | 5.0-10.3 | 0-6.7 | 0.9-6.7 | 0.1-6.9 |
| 9 | | | | | 0.9 | 0.6 | 4.4-11.4 | 0-6.7 | 0.4-6.0 | 0.1-6.0 |
| 10 | | | | | 1.2 | 0.3 | 4.6-10.8 | 1.6-8.3 | 0.4-6.0 | 0.1-6.0 |
| 11 | | | | | 1.6 | 0.2 | 4.3-10.1 | 0-6.7 | 0.0-2.0 | 0.1-3.2 |
| 12 | | | | | 0.0 | 0.0 | 4.3-10.1 | 0-6.7 | 0.4-3.4 | 0.1-3.8 |
| 13 | | | | | | | 0.9-8.8 | 0-5.8 | 0.4-3.4 | 0.1-3.8 |
| 14 | | | | | | | 0.9-8.8 | 0-5.8 | 0.1-4.3 | 0.1-3.1 |
| 15 | | | | | | | 1.2-8.2 | 0-5.0 | 0.1-4.3 | 0.1-3.1 |
| 16 | | | | | | | 1.2-8.2 | 0-5.0 | 0.0-4.8 | 0.0-2.7 |
| 17-18 | | | | | | | 1.8-8.3 | 0-5.8 | | |
| 19-20 | | | | | | | 2.9-8.6 | 0-6.6 | | |
| 21-22 | | | | | | | 1.5-6.5 | 0-4.1 | | |
| 23-24 | | | | | | | 1.7-5.5 | 0-4.1 | | |
| 25-26 | | | | | | | 1.3-6.6 | 0-3.3 | | |
| 27-28 | | | | | | | 1.4-6.3 | 0-3.3 | | |
| 29-30 | | | | | | | 0.4-5.2 | 0-2.5 | | |
| 31-32 | | | | | | | 0.4-4.8 | 0-2.5 | | |
| 33-34 | | | | | | | 0.5-4.5 | 0-1.7 | | |
| 35-36 | | | | | | | 0.1-3.7 | 0-1.7 | | |
| 37-38 | | | | | | | 0.2-3.3 | 0-0.9 | | |
| 39 | | | | | | | 0.2-2.7 | 0-0.1 | | |

* Before and After the Application of Standard Fault Coverage
** CADAT and HITS ONLY

# 4. RECOMMENDATIONS

## 4.1 INTRODUCTION:

It was noted in the previous chapter that the intent of this study was to obtain a better correlation of the four simulators. To do that, each simulator was studied in terms of its fault handling techniques, fault injection, fault collapsing, classing, fault coverage evaluation, etc. (Chapter 2). Then, different test circuits (combinational and sequential) were simulated on these fault simulators and the results were observed and analyzed (Chapter 3). Although, it was not obvious how to suggest better correlation among the simulators, it was clear that the method of fault classing was the common ground among them. Hence, we recommend to re-evaluate the fault coverage on the basis of this observation as will be stated below. That would require each simulator to follow a standard procedure for fault classing. For the most part, faults are classified similarly, however, some changes have to be used for some simulators since they either add or delete certain classes because of their assumptions. These differences will also be noted.

In addition, when primitives do not exist in certain simulators and macros are built and used instead, the same faults must be injected and hence some guidelines are given to address this case. Some guidelines will also address the way testing must be done when a clock or control input is used since simulators tend to define and use such signals differently. The following section will discuss in details these recommendations and guidelines.

## 4.2 RECOMMENDATIONS AND GUIDELINES FOR BETTER CORRELATION OF FAULT SIMULATORS

The following guidelines must be followed in evaluating fault simulators. These guidelines apply in some parts to the specific simulators used in this study. However, the main recommendations

are generic enough that any simulator can be made to adhere to the basic recommendations given below. The MOE figure should give the indication on how far or close any two or more simulators are from each other. In other words, whether or not these simulators are close or far in their way of fault injection, classing, and coverage evaluation.

Hence, the following is the guidelines recommended for fault simulator evaluation.

GUIDELINE 1:

**Use the same circuit structure (topology) (nodes, gates, blocks, interconnections, etc.), and same ordered test patterns (vectors).**

If a different topology is given, then in turn, a different fault injection and classing techniques is used and hence the correlation is made more inconsistent. Similarly, if the test vectors are different or ordered differently (especially in sequential testing) the results will be harder to correlate.

GUIDELINE 2:

**Use fault classes as basis for evaluating the fault coverage. In other words: define a standard fault coverage as:**

$$\text{Fault Coverage (F.C.)\%} = \frac{\text{\# of Detected Fault Classes}}{\text{Total \# of Fault Classes}} \times 100$$

This is the basic finding in this study, since it was found that fault classing and equivalencing techniques are very similar in many simulators, while fault injection may be quite different as was shown in the previous chapter. In addition, one may get an optimistic number in evaluating fault coverage using the total number of faults since many faults are equivalent. When the

standard fault coverage was used, the fault coverage among all simulators was much closer as illustrated in the test circuits.

However, it was mentioned that some simulators change the number of classes due to certain assumptions inherent to the simulator. These assumptions must be taken out so that each simulator can be as close to the standard as possible. These rules are given below for each simulator used in this study.

a) CADAT:

CADAT adds 2 classes (s/0 and s/1) to each primary input which has no fanout as was shown in Chapter 2. Hence, the number of classes in CADAT will always be greater than the standard. These extra classes are equal to: # of PI with no fanout points x 2 (s/0, s/1). Hence, **these classes must be identified and removed from the class detection list**. This rule was used in achieving all standard fault coverage in the test cases as stated earlier.

b) HITS:

HITS adds 2 classes (s/0 and s/1) to each primary output which has a fanout. This case was illustrated earlier in the edge-triggered D FF example. **These classes must be removed so that HITS can conform to the standard calculation**. This is true in the case of CMOS, however, in the case of TTL only one extra class is added (s/1) as explained in Chapter 2.

In addition, it was observed that HITS was the only simulator that removes faults due to technology. Although, these assumptions are very reasonable, **one has to declare the CMOS technology when using HITS** so that roughly the same number of faults are injected and a better correlation is arrived at. While nothing can be done about it, one has to be aware that when HITS is used, the flip-flop outputs s–a–o faults are classified with the clear line being s–a–0. This functional equivalence is correct but not used in any other simulator. It was observed that the difference, however, is not significant.

c) HILO:

HILO does not have a large library of primitives, and hence when a primitive is used, one has to build a macro in its place. The simulator does not inject any faults at the macro boundary and therefore some faults and consequently fault classes are omitted. To overcome this case, **a buffer is inserted at each PI of the macro** as shown in Fig. 4.1. These buffers will allow for the injection of faults at the PI lines.

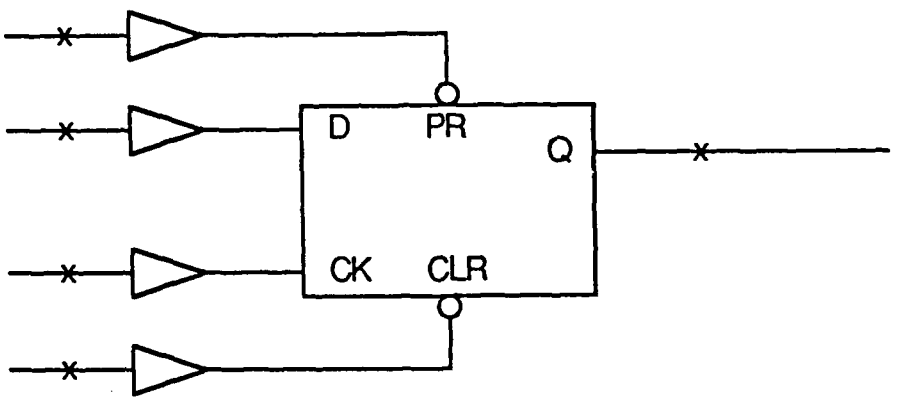
d) LASAR:

LASAR has the same condition as HILO and **buffers can be used**. However, if no buffers are used, all internal faults to the flip-flops are injected which is in return considered in the total evaluation. Depending on whether or not the test vectors detect these added faults, the Fault Coverage may be less or more than the standard. LASAR provides two options for fault injection and evaluation. At the moment, there is no easy way of not injecting these internal faults to arrive at a common correlation. Therefore, if buffers are used, the total number of classes may have to be computed by hand through the fault dictionary (all internal classes to macros may have to be removed by hand). In some instances, some faults are not detected when applying Efaults simulator, these undetected faults have to be entered individually through Faultput simulator. However, Faultput does not provide any information pertaining to classes. Furthermore, **if only chips are used and all internal faults are considered in all simulators, then a common correlation can be obtained.**

GUIDELINE 3:

**Evaluate the correlation factor among simulators; the Margin Of Error (MOE) percentage as:**

**The range between the minimum difference between any two simulators and the maximum difference between any two simulators.**




( x : fault injection )

Fig. 4.1 Inserting Buffers to PI's

This number is evaluated at the end of the test vectors using the final standard fault coverage of the network. One must decide, however, on the acceptable number of correlation. This figure of merit, in our test cases, when all conditions are normalized and unknown errors removed, ranged from 0 to 1.8%, which is relatively a good acceptable range.

GUIDELINE 4:

**In sequential circuit simulation, the following Apply (test)/Read(Sense) pattern is most effective. This guideline is important so as not to leave it to the user on when to apply the test patterns and observe the response but rather all simulators will use the same procedure.**

(a) **For negative edge cells:** Apply the test vector before the negative edge of the control input (or clock), sense the output (after propagation delays) after the control input is back to zero, and sense it again when the control input is back to 1 (after propagation delays) as shown in Fig. 4.2(a).

(b) **For positive edge cells:** Apply the test vector before the positive edge of the control input, then read the output when the control input goes to 1 (after circuit propagation delays) and read again when the control input goes back to zero and before applying the next test vector as shown in Fig. 4.2(b).

This procedure is found to be very effective in detecting more faults per step in the simulation. This procedure must also be programmed in the ATE system. The ATE system performs tests on physical devices with electrical parameters that may have not been observed during simulation. The ATE system performs simple judgements, usually PASS/FAIL in nature as programmed. Thus, it must be supplied with inputs to present to the device under test, and consequently it must be told what to expect from the device as a result.

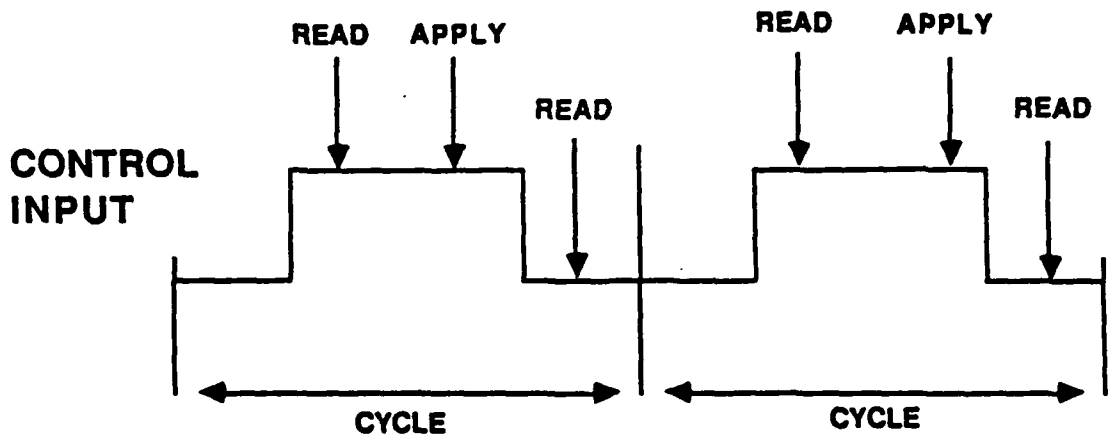



Fig 4.2(a) Negative Edge Cell

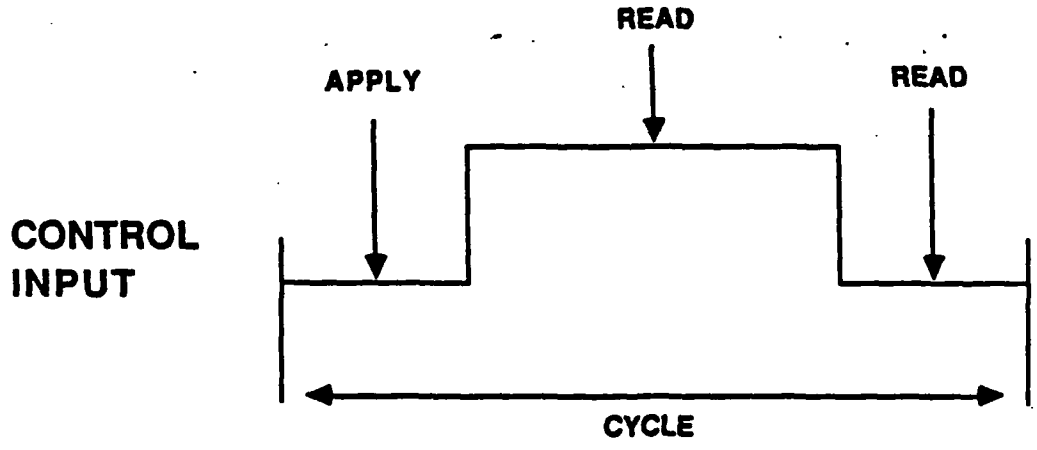



Fig 4.2(b) Positive Edge Cell

Fig. 4.2 Method of Applying Test Vectors and Sensing Outputs

OBSERVATION: In addition, for the given simulators, **the following rules were applied for test application on the control inputs or clock lines.**

(a) CADAT: Two methods may be applied (not both):
   1) Use buffers and read (sense) twice in a cycle; one before the buffer (input) and one after it (output of buffer) **or**
   2) Apply two test vectors and read twice (when control input is high and when control input is low). These are the only two ways that could be applied since CADAT does not allow reading twice in one cycle.

(b) LASAR: Open windows at reading times, since LASAR allows sensing outputs at any time.

(c) HILO: Read twice per control input or clock cycle. This is valid in HILO.

(d) HITS: Apply control input 3 times (101 or 010) and observe response every time One must also note that if a combinational gate has a PO in HITS, more coverage per step may be obtained due to response during the apply phase (reading three times instead of two). However, they can be applied to the same cycle.

GUIDELINE 5: **X-propagation and Potential (Possible) Detects**

Several techniques for X-propagation handling and possible (potential) faults can be applied so that only solid faults can be detected. The source of potential detects is open-collector outputs in combinational networks and clock lines in sequential circuits when it is not possible to internally intialize the flip-flop.

OBSERVATION: The following observations are made in connection with potential detection handling:

(a) Open-collector faults and Ground (or Vcc) faults: These types of faults produce potential faults in CADAT and LASAR, are not considered at all (removed from the fault list) in HITS which in turn gives an optimistic coverage, and in HILO, where open-collector faults are considered solid (Weak High) and ground faults are removed (undetectable).

(b) One can change the potential detection to solid detection in sequential circuits as follows:

i) If a path exists, intialize internal FFs.

ii) Use design for testability techniques (DFT), if possible, by adding two pins to initialize all internal FFs simultaneously (CLR and PR lines).

iii) Else, the clock line will always (or most of the time) be declared potential detects. However, in practical *situations and with multi-output systems*, one may do the following as far as the clock line is concerned:

1) Observe values of outputs before applying the vectors (no longer indeterminate values).

2) Apply some vectors with CK pulse, then observe outputs, if there are no changes in the output response then, CK faults can be declared solidly detected.

(c) **Guideline for Clock lines:**

In general, if I/0 lines of the clocked device are solidly detected, one could give credit for possible detects for clock line faults.

## 4.3 CONCLUSION

The objective of this task was to use digital gate level simulation packages in designing and testing VLSI microcircuits. A practical measure of testability is the fault coverage achieved by fault simulators. Since specific levels of fault coverage frequently are contractual requirements in system design, there is a need to be able to relate fault simulation results from many simulators to an acceptable standard. Here, five guidelines are proposed to be used as a standard. The major two rules are the way the fault coverage is evaluated and the way the margin of error is calculated. Both of these values are related as was shown in the test circuits, and if these recommendations are adopted, a better correlation among the different fault simulators is achieved.

# 5. FUTURE CONSIDERATIONS

The software supports needed for testing are programs for using computers to generate test-patterns, evaluate test-results, and control test-equipment for automated testing. Most types of test-software supports are programs for: test generation, fault simulation and test verification, fault diagnosis and testability analysis. Fault simulators model the circuit behavior in the presence of faults. With the presence of the proposed rules or guidelines a more coherent correlation between different simulators can be obtained as also mentioned in [11].

Furthermore, these guidelines must be tested on other simulators to reinforce the generic nature of these guidelines.

Other considerations may include timing analysis on these simulators, testability analysis, behavioral simulation, A/C (delay) and transition fault insertions [12], switch-level simulation, hardware accelerators [13], and the impact of design for testability techniques [10]. Finally, it may very well prove to be an excellent idea if a standard is proposed for fault injection or fault classing that all simulators can conform to. For example, fault classes could be defined in a standard form and hence, all simulators will then conform to this standard. This should make it relatively easy since fault classes are very simlar. If such a standard is achieved, it becomes much easier to compare (or correlate) the different simulators. However, such a standard, may prove difficult to enforce although the quality assurance and reliability engineers may find it to their advantage.

# REFERENCES


[1] Miczo, Alexander, Digital Logic Testing and Simulation, Harper and Row, N.Y., 1986.

[2] Parker, Kenneth, Integrating Design and Test: Using CAE Tools For ATE Programming, Computer Society Press, IEEE, Wash. D.C., 1987.

[3] Williams, T. W., Editor, VLSI Testing, North-Holland, Elsevier Science Publishers, N.Y., 1986.

[4] Tsui, Frank, LSI/VLSI Testability Design, McGraw-Hill Co., 1987.

[5] Lala, P., Fault Tolerant and Fault Testable Hardware Design, Prentice-Hall Int., New Jersey, 1985.

[6] Agrawal, V., and S. Fung, "Multiple Fault Testing of Large Circuits by Single Fault Test Sets," IEEE Transactions on Computers, Vol. C-30, No. 11, Nov. 1981, pp. 855-865.

[7] Wadsack, R., "Fault Modeling and Logic Simulators of CMOS and MOS Integrated Circuits," Bell System Technical Journal, Vol. 5, May-June 1978, pp. 1449-1473.

[8] Al-Arian, S., and D. Agrawal, "Physical Failures and Fault Models of CMOS Circuits," IEEE Transactions on Circuits and Systems, Vol. CAS-34, No. 3, March 1987, pp. 269-279.

[9] Computer Design, "Buyers Guide to PCB Simulation Systems," June 16, 1988, pp. 93-103.

[10] Fujiwara, Hideo, Logic Testing and Design for Testability, The MIT Press, MA., 1985.

[11] Harbert, T., "Military sets goal for JAN approval," EDN News, Feb. 1988, pp. 27-28.

[12] Waicukauski et al, "Transition Fault Simulation," IEEE Design and Test of Computers, April 1987, pp. 32-38.

[13] Smith, David, "Finding Fault: An Update on Fault Simulation," VLSI Systems Design, October 1987, pp. 28, 29, 34 & 65.

# APPENDIX

## TEST VECTORS

XNOR
====

```
-------------
INPUT  A, B
-------------
00B
01B
10B
11B
=============
```

2 - BIT ADDER
=============

```
----------------------
INPUT  A0,A1,B0,B1,C0
----------------------
00111B
01001B
00011B
11000B
10100B
01110B
======================
```

GRAY
====

```
--------------------------------------
INPUT I1,I2,I3,I4,I5,I6,I7,I8,GROUND
--------------------------------------
000000000B
101010101B
110101011B
011111111B
======================================
```

## 4 - BIT COMPARATOR 7485

```
-------------------------------------------------
INPUT AGTBIN,AEQBIN,ALTBIN,A3,A2,A1,A0,B3,B2,B1,B0
-------------------------------------------------
001111111111B
011000100000B
110000000010B
100111011110B
011010000000B
011100000000B
110000000001B
011001000000B
110000001000B
110000010000B
010000000000B
000000100001B
000000100010B
000000101000B
000000110000B
000001000001B
000001001000B
000001010000B
000010000001B
000010000010B
000010010000B
000100000001B
000100000010B
000100001000B
=================================================
```

## ALU 74181

```
-------------------------------------------------
INPUT  S3,S2,S1,S0,B3,A3,B2,A2,B1,A1,B0,A0,M,CI
-------------------------------------------------
011000110110018
100111000001118
110100011000008
011011000000018
011001101101018
100101010110008
101010001011008
010110010011018
100011100100108
000101100100008
010011111101018
100000111100008
000001000101008
000001010001008
010011010000008
=================================================
```

EDGE-TRIGGERED DFF

```
==================
-----------------
INPUT NPR,D,NCLR
-----------------
111B
110B
101B
100B
011B
010B
001B
=================
```

TWO-DFF + AND

```
-----------------
INPUT  NPR,NCLR,D
-----------------
001B
100B
101B
111B
111B
110B
110B
=================
```

```
4 - DFF CASCADED
================

----------------
INPUT D,NPR,NCLR
----------------

D,NCLR = HI
NPR = HI,LO,HI
NCLR = HI,LO,HI

111B
111B
111B
111B

D = LO;
NCLR = HI,LO,HI $
NPR = HI,LO,HI $

011B
011B
011B
011B
011B
================
```

```
        COUNT163
        ********

--------------------------
INPUT CLR,LD,EP,ET,A,B,C,D
--------------------------
8FH
FFH
8BH
3FH
8CH
CFH
F0H
8FH
EEH
8BH
B0H
8FH
DFH
87H
F0H
8DH
F0H
8EH
70H
8BH
F4H
81H
E4H
8EH
FAH
80H
F0H
86H
F0H
84H
F0H
8AH
F0H
83H
F0H
89H
F0H
8DH
D0H
**************************
```

## 4- BIT SHIFTER 74195

| INPUT A,B,C,D,S/L,J,KH,CLR |
|---|
| F7H |
| 00H |
| 01H |
| FEH |
| F6H |
| 60H |
| 0CH |
| 55H |
| AAH |
| F4H |
| FCH |
| 44H |
| 4CH |
| 32H |
| 82H |
| 0EH |

# *MISSION*
# *of*
# *Rome Air Development Center*

*RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control, Communications and Intelligence ($C^3I$) activities. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of $C^3I$ systems. The areas of technical competence include communications, command and control, battle management information processing, surveillance sensors, intelligence data collection and handling, solid state sciences, electromagnetics, and propagation, and electronic reliability/maintainability and compatibility.*